High-Ohmic Resistors using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers

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ESSDERC 2013

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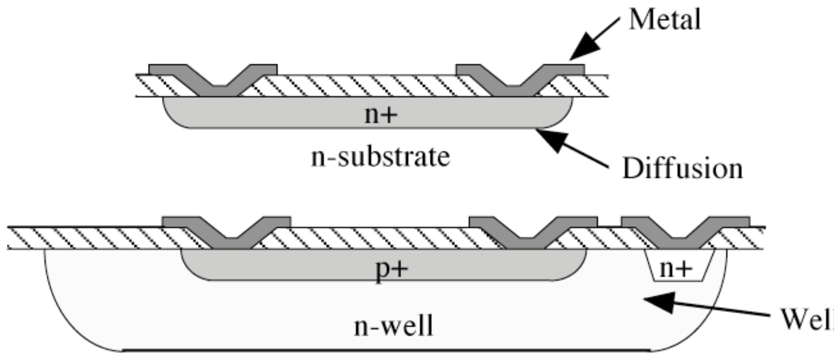
Outline

- Introduction to integrated resistors
- PureB-layer integration in $p^{+}n$ diode applications
- PureB-layer resistor process flow
- Test structures and qualification parameters
- Electrical measurement results
- Conclusions

Introduction to integrated resistors

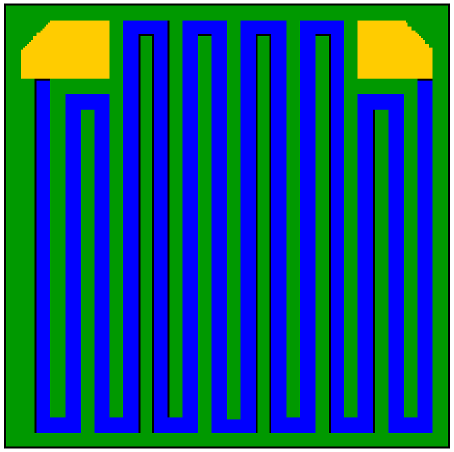
Most commonly used integrated resistors: **diffused / implanted p- or n-type regions**

- Resistance values ~ 1 Ω – 10 kΩ:
  - straightforward to integrate
  - sheet resistance values ~ 10 -1000 Ω/□
  - depletion of resistor doping minimal
  - small resistor biasing dependence
  - small parasitic junction capacitance



[www.eet.bme.hu/~benedek/VlsiDesign/Lectures]

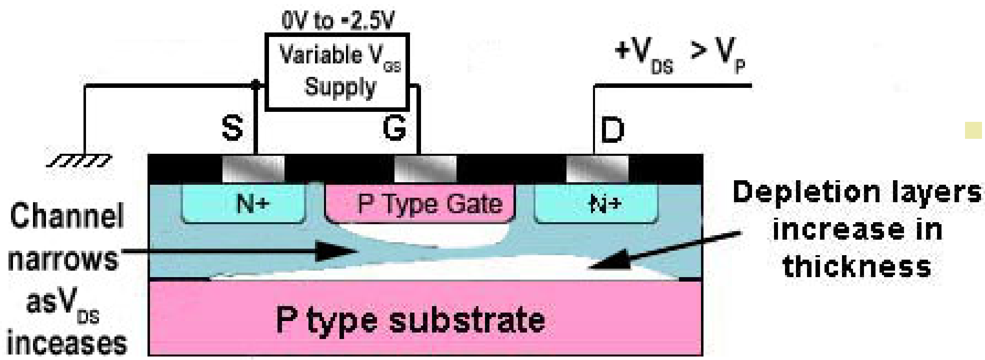
- Resistance values > 100 kΩ:
  - with low sheet resistance
    - × long meander resistors necessary
    - × large parasitic capacitance
  - with high sheet resistance (~ 10 kΩ/□)
    - × high bias dependence
    - × poor doping reproducibility



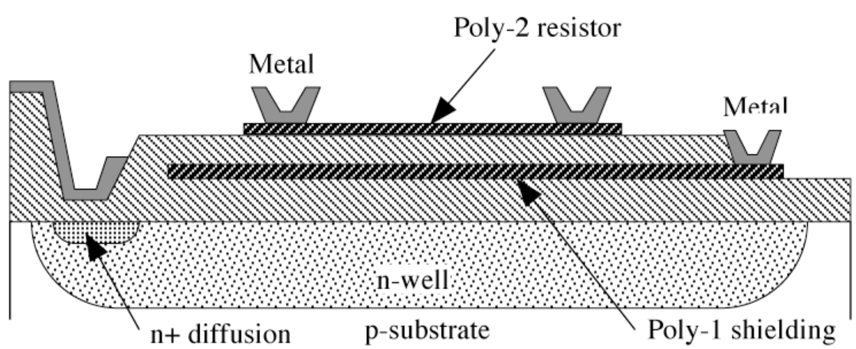
[www.semiconwell.com]

Introduction to integrated resistors

Common solutions for mega-ohm resistor integration



[www.learnabout-electronics.org/fet_02.php]



Combination of negative (polySi) and positive (c-Si) TCR resistors used to lower overall TCR. Due to process variations in both materials this is a low-yield solution. [N. Sadeghi, CCECE 2011]

- Pinched resistors:
  - straightforward to integrate
  - sheet resistance values ~ 30 kΩ/□
  - small parasitic junction capacitance
  - ✗ bias dependent

- Polysilicon resistors:
  - lightly-doped deposited poly-silicon on oxide layer
  - ✗ non-uniform resistor value over the wafer
  - ✗ charging/discharging of defect states
  - ✗ oxide interface states cause variable resistance values

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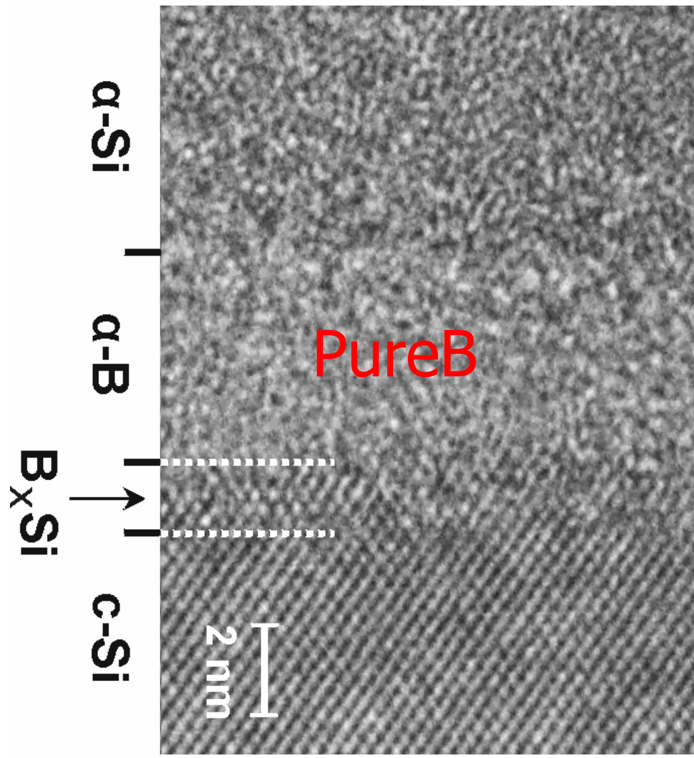
Pure boron chemical-vapor deposition

- CVD parameters:
  - epitaxial Si/SiGe CVD reactor
  - gas source: diborane (B_2H_6)
  - Carrier gas : hydrogen (H_2), (N_2)
  - temperatures: 500 to 700 ºC
  - lower temperature /diborane partial pressure ➔ slower formation of PureB layer
  - constant slow growth rate, nm/min

- Properties of PureB layer:
  - high resistivity of ~ 10^4 Ω-cm
  - chemically robust
  - does not oxidize or change in time
  - is resistant to many standard cleaning procedures

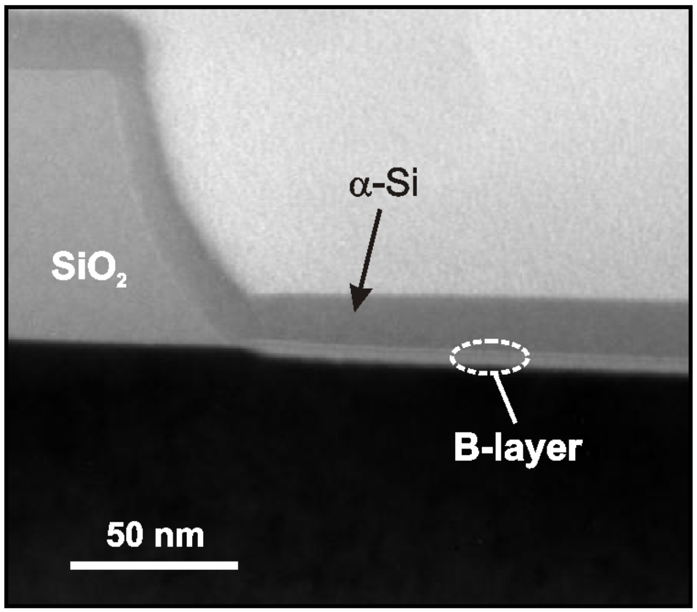
HRTEM of 700°C deposition:



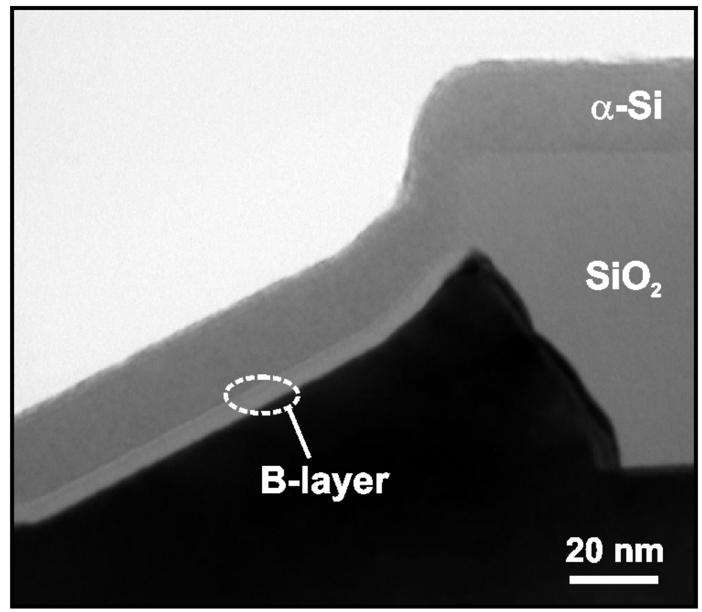
Other PureB deposition properties

Under the right conditions:

- at 700ºC high selectivity to native-oxide-free Si surfaces
- uniform depositions for temperatures: 400ºC – 700ºC
- isotropic deposition on Si



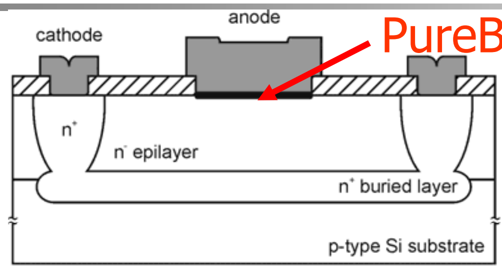
Uniform coverage



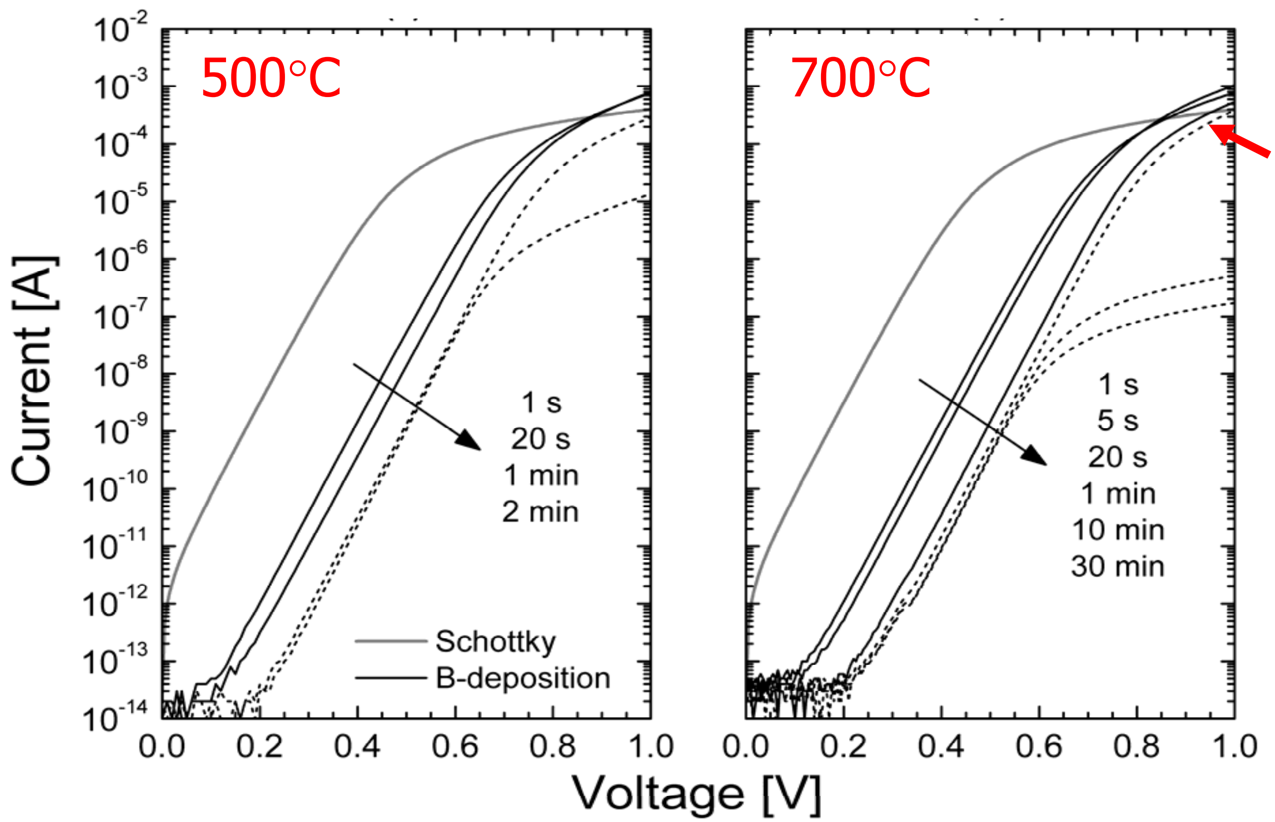
Isotropic deposition

Sarrubi, JEM 2009

PureB p^+n forward diode characteristics



p^+n diodes with n-doping ~ 10^{17} cm^{-3}



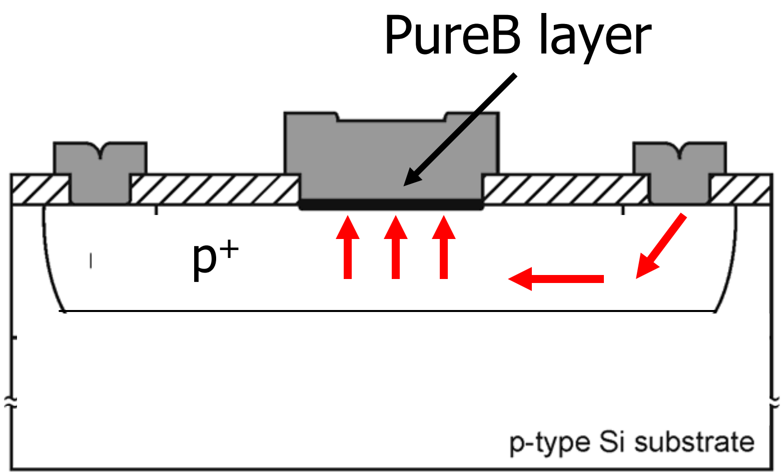
Same behaviour for both deposition temperatures.

Behaves like conventional deep p^+n junction:

near-ideal with low saturation current

Sarubbi, IEEE-TED 2010

Vertical resistance



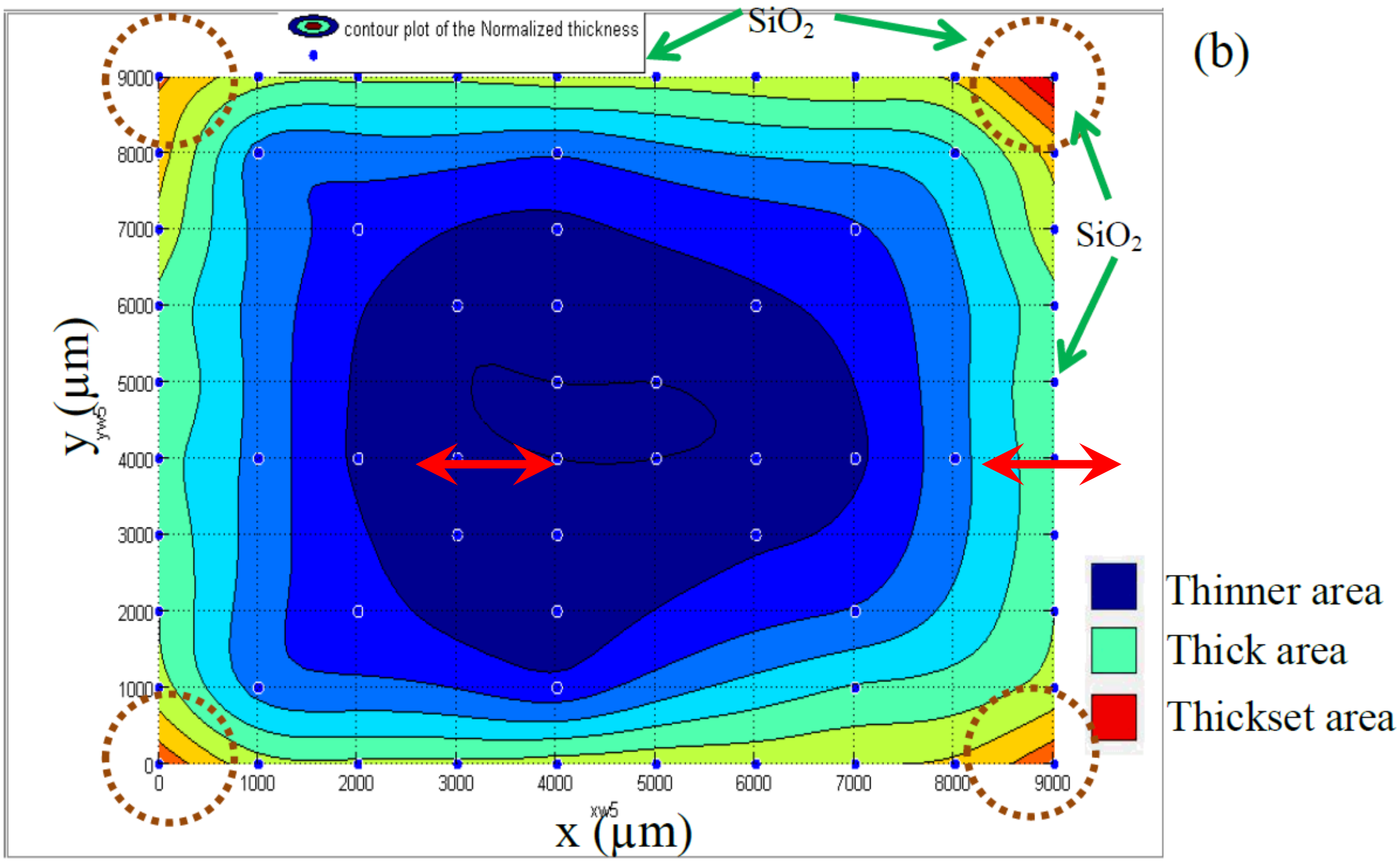
Can use PureB layer as a vertical resistor:

- linear resistance on p-type Si
- resistivity very high but varies from run to run: 500 - 10^4 ohm-cm
- easily make small mega-ohm resistors

The very high resistivity of the bulk PureB layer means that it does not play a role for the lateral sheet resistance. This is dominated by doping of the Si (700°C) or the PureB/Si interface properties (500°C).

Deposition loading effects influence thickness

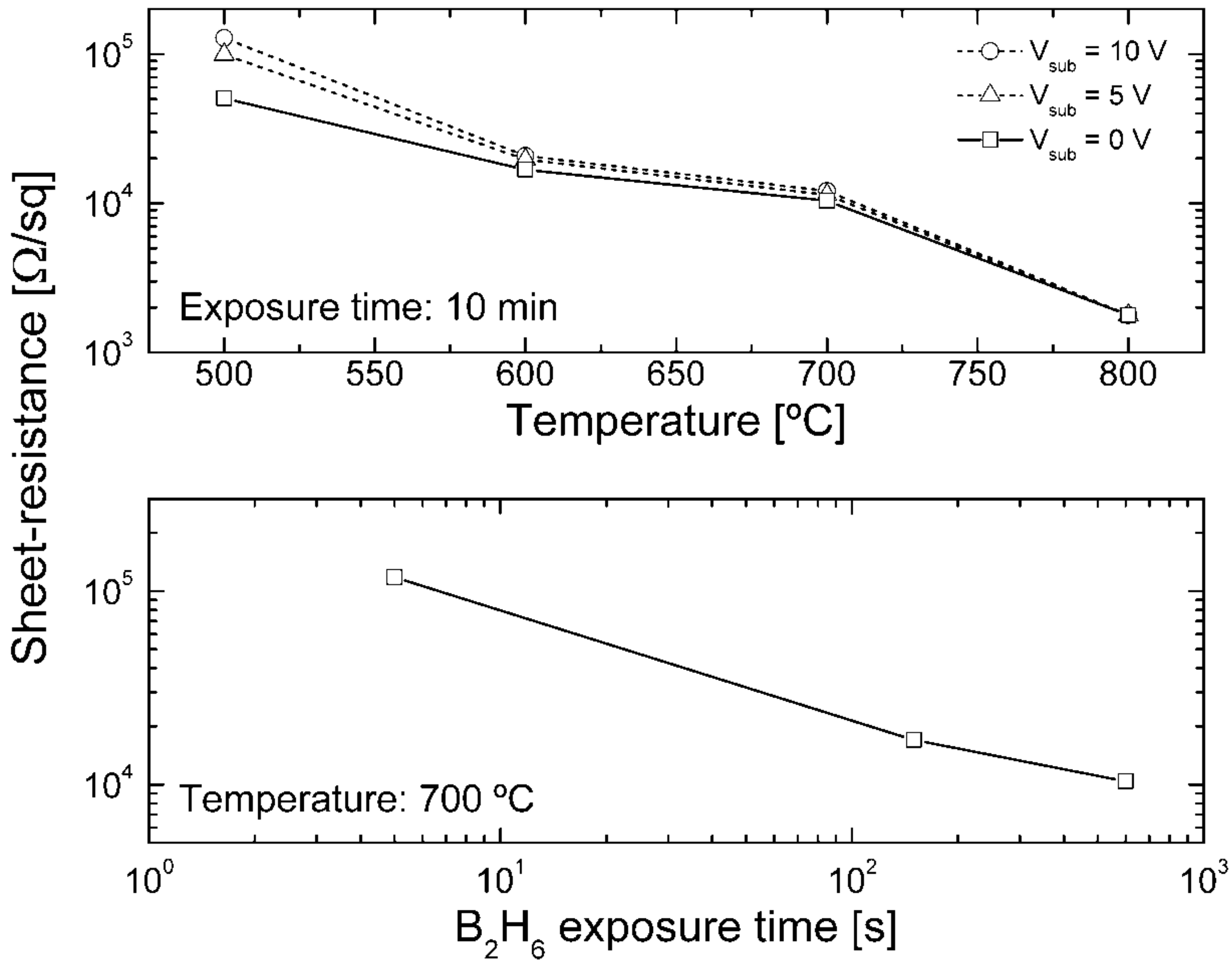
Pattern-dependent thickness control ⇒ poor vertical resistance control



Measured photodiode responsivity of low-energy electrons in e-beam set-up

[V.Mohammadi, ECS-JSSST 2012]

Sheet resistance measurements



~ 100 kΩ/□ for low-temperature deposition or short- time deposition

Substrate doping ~ 10^{15} cm^{-3}
- bias dependence saturates

solid solubility of B in Si at 700°C = $2x10^{19}$ cm^{-3}

Sarubbi, IEEE-TED 2010

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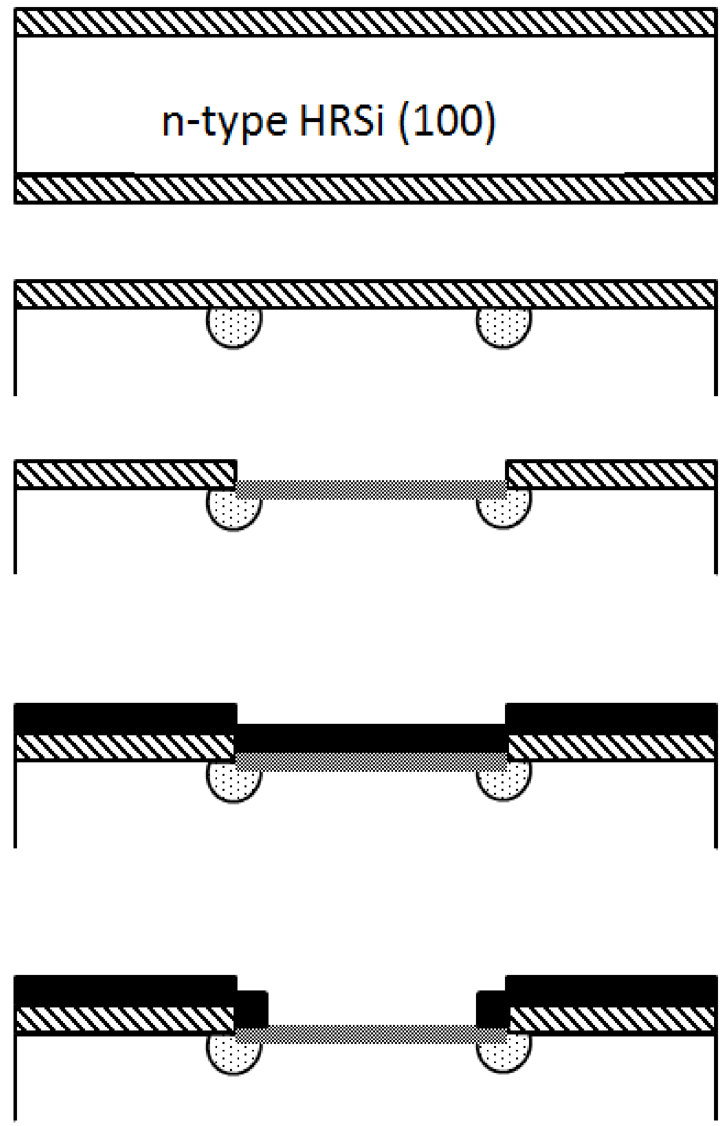
PureB-layer resistor process flow

1) High-resistivity Si (HRS) <100> wafers n-type phosphorous-doped to 2-10 kΩ-cm
2) 200 nm thermal oxide
3) optional p-type B^+ implanted guard ring / contact
4) window opening and PureB deposition, ~ 3 nm at 700°C or 500°C
5) 1000 nm Al deposition
6) Al dry etching with wet landing on PureB with diluted HF dip
7) Alloying in forming gas 400°C 30 min



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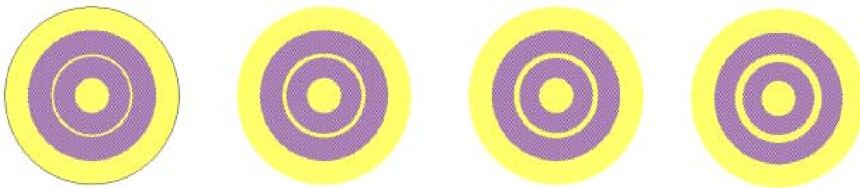
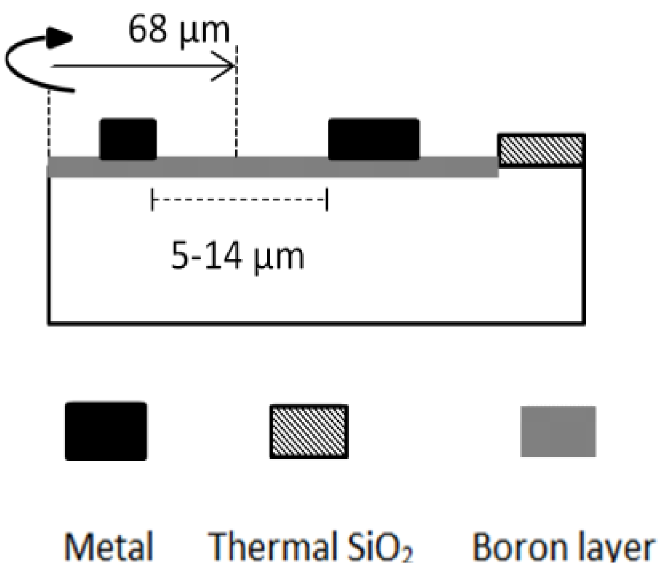
Sheet resistance measurement structures

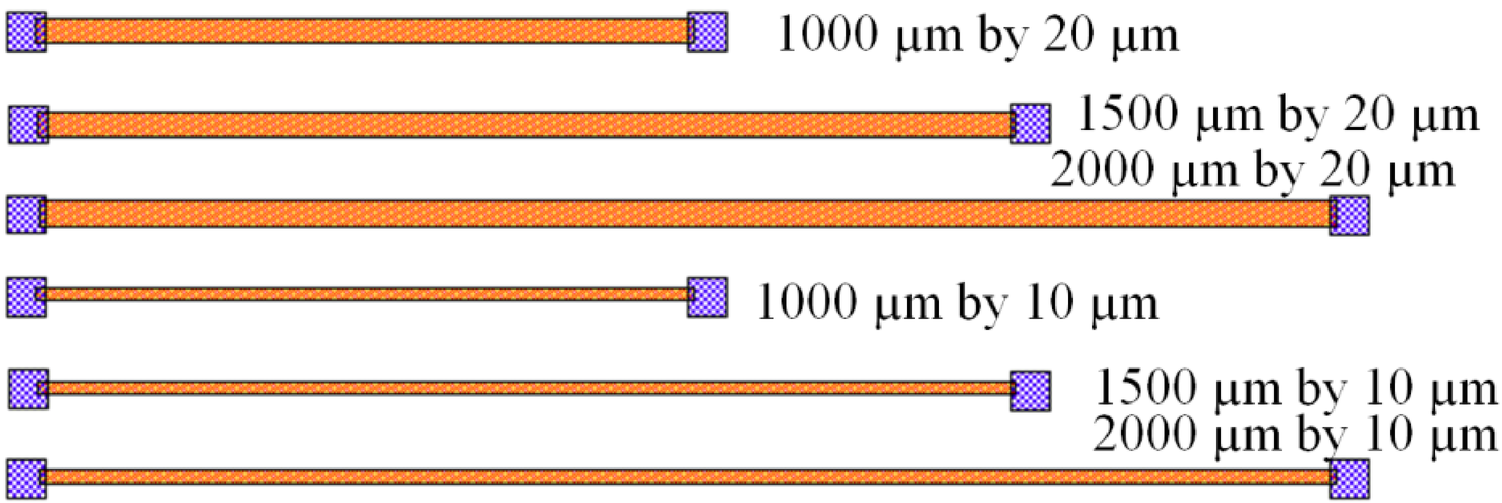




PureB layer deposition conditions	Sheet resistance
7-min 700ºC	2.5×10^{4} Ω/□
20-min 500ºC	3.8×10^{5} Ω/□

Resistor geometries

Selection of the measured resistors



Resistor qualification parameters

- **Resistor tolerance TR** (permissible deviation from the nominal value at 25°C) is evaluated from over the wafer measurements of the average resistance *Rav* inserted in the equation:

$$TR(\%) = \frac{Ri - Rav}{Rav} \times 100$$

- **Resistor voltage coefficient resistors VCR**: change in resistance with applied voltage

- **Resistor temperature coefficient TCR**: change in resistance with temperature

$$TCR\left(\frac{ppm}{°C}\right) = (10^6)\frac{R - Ro}{Ro(T - To)}$$

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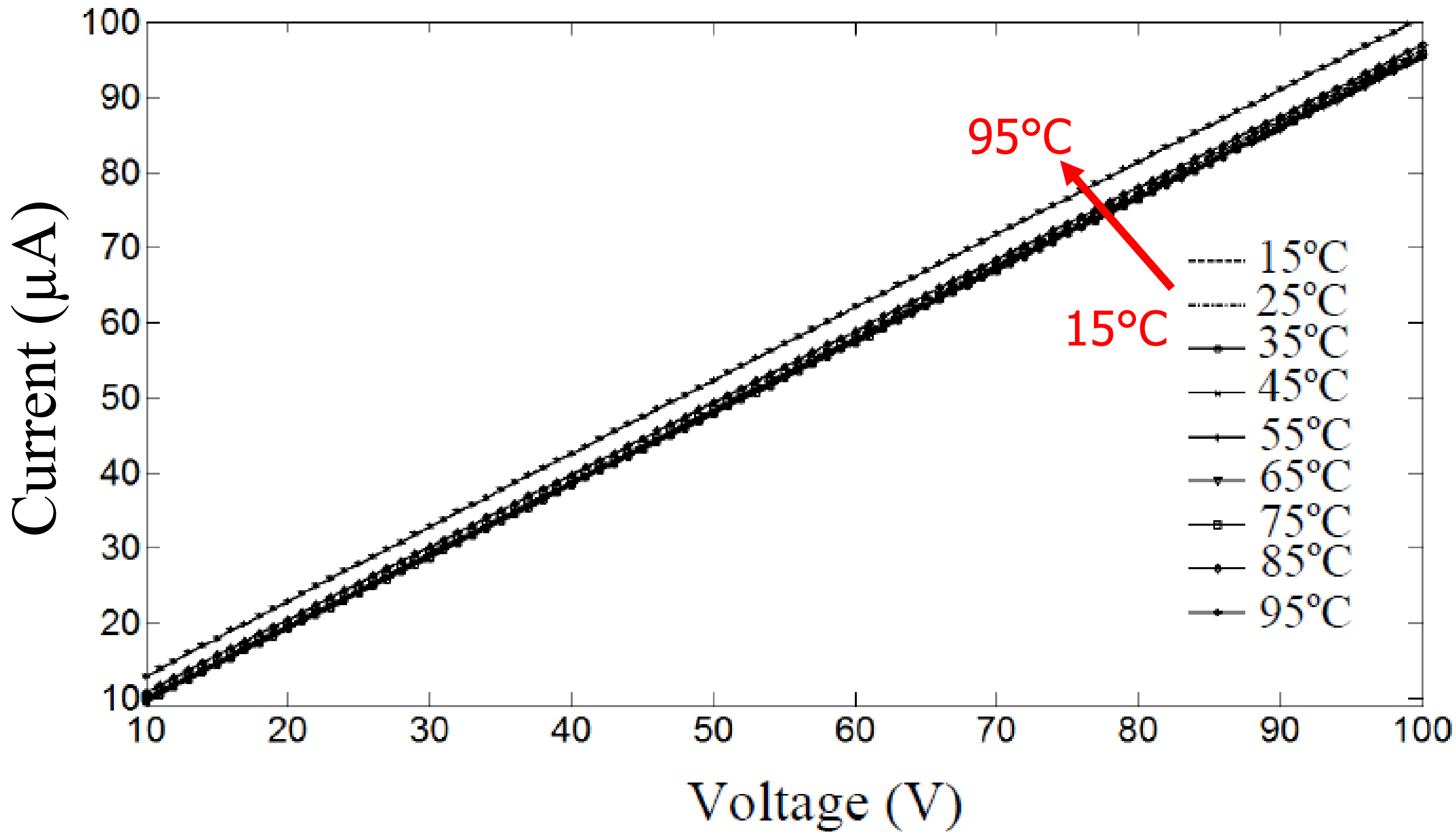
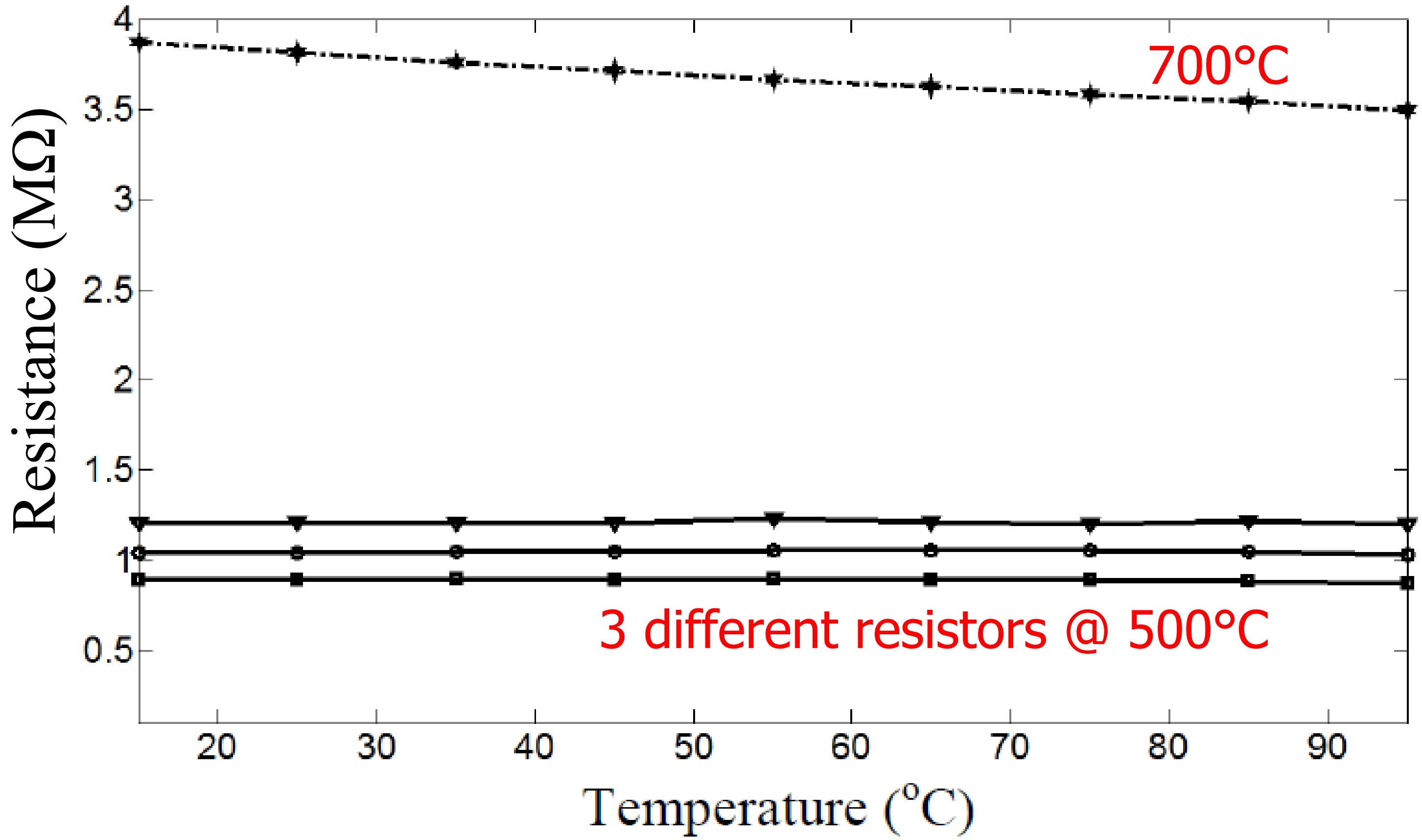
I-V characteristics of 700°C resistors

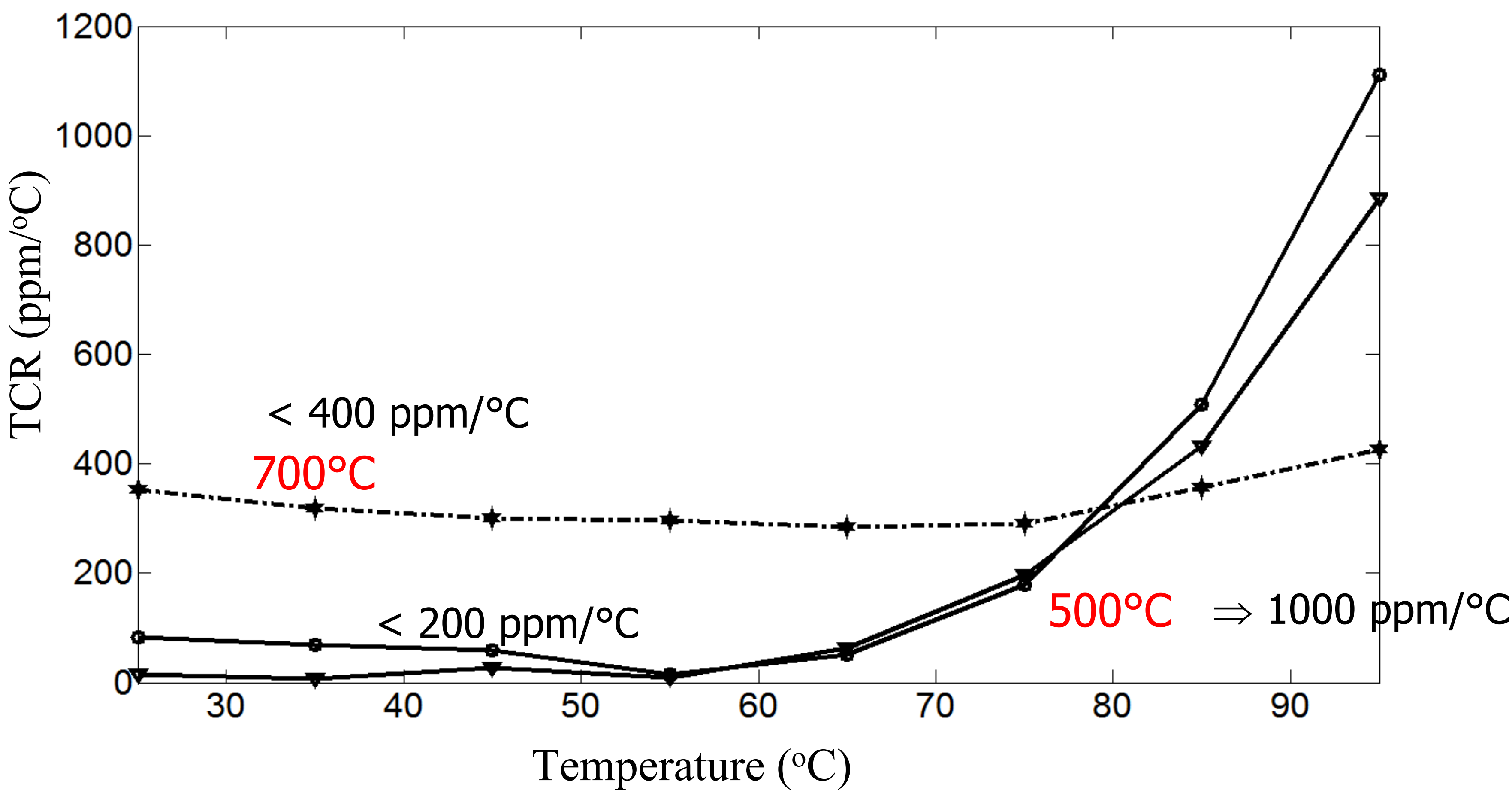
Highly linear I-V relationship ⇒ VCR ~ 0
From 85°C to 95°C the resistance value decreases slightly.
Stable under temperature cycling.
Diode leakage < $1 nA/cm^2$.



Temperature dependence of resistance



Temperature coefficient of the resistors



Resistor tolerance

Examples of the tolerance of the fabricated PureB resistors

R(Ω) / Die	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	R5 (MΩ)	R6 (MΩ)	R7 (MΩ)
Die 1	20	23	307	872	1.023	1.45	3.82
Die5	21	23.1	308	874	1.11	1.59	3.78
Die12	20	23	304	875	1.09	1.49	3.87
Average	20.3	23.03	306	873.6	1.07	1.51	3.82
Tolerance	3.2%	0.3%	0.7%	0.2%	3.3%	5.3%	1.2%

Conclusions

PureB resistors can be fabricated with

- sheet resistance values up to the 100 kΩ/□ range depending on deposition temperature/time in the range 500°C to 700°C,
- high linearity for all deposition temperatures,
- exceptionally low TCR, e.g. 400 ppm/°C from 15°C to 95°C, for mega-ohm resistors
- front-end CMOS compatible processing,

  the PureB layer can be covered with a dielectric for protection and/or increased integration compatibility.