Flicker Noise in Advanced CMOS Technology: Effects of Halo Implant

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Outline

- Motivation
- Flicker Noise and Unified Flicker Noise Model
- Measurements
- Model
- Verification
- Discussions
- Conclusions

Motivation: System On Chip

digital CMOS

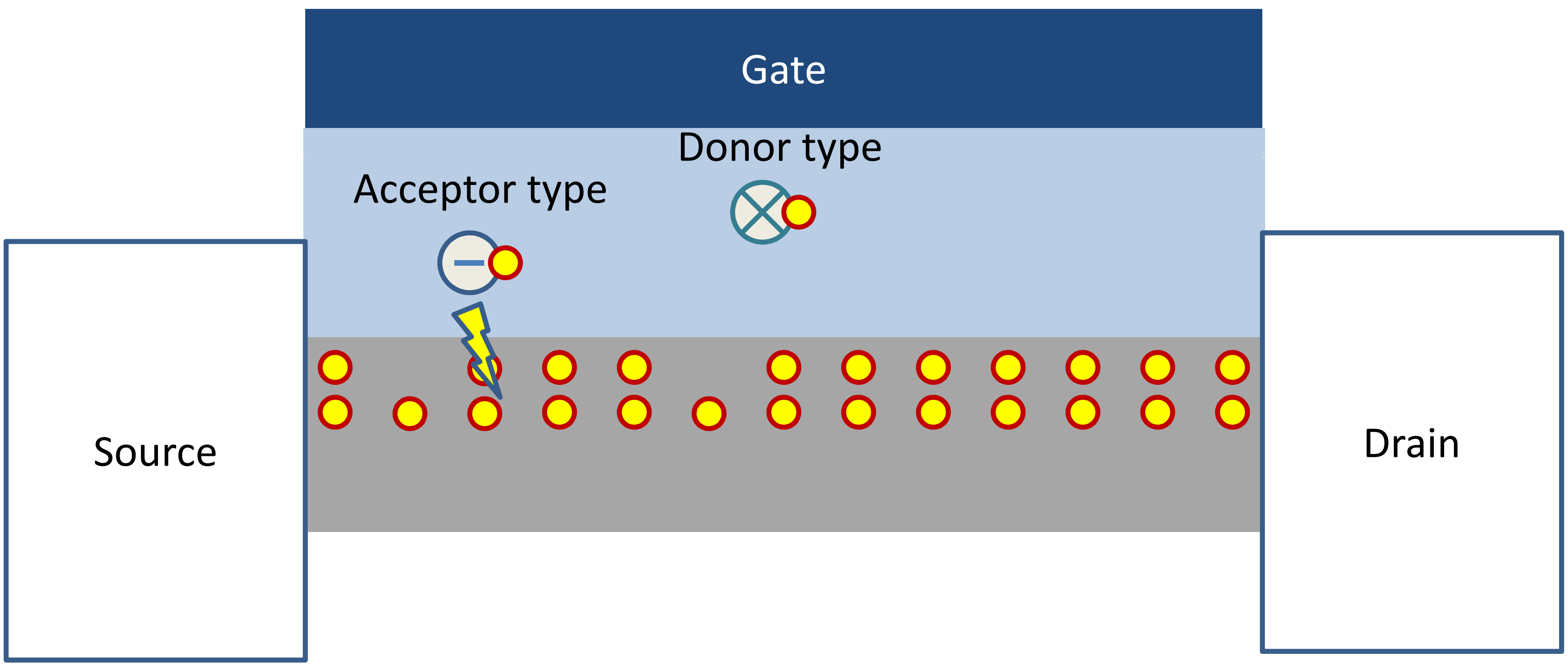
- Short Channel Effects

RF CMOS

- Noise

Flicker (1/f) Noise

- Flicker noise: the fluctuation of drain current due to Oxide Traps:
    1. Reduction in channel carrier density
    2. Change in mobility due to Coulomb Scattering



Unified Flicker Noise Model

- The unified drain-current FN power density as a function of frequency f

$$S_{\text{ID}}(f) = \frac{k_B T I_d^2}{\gamma f W L^2} \int_0^L \frac{N_t^*(E_{\text{fn}})}{N(x)^2} dx$$

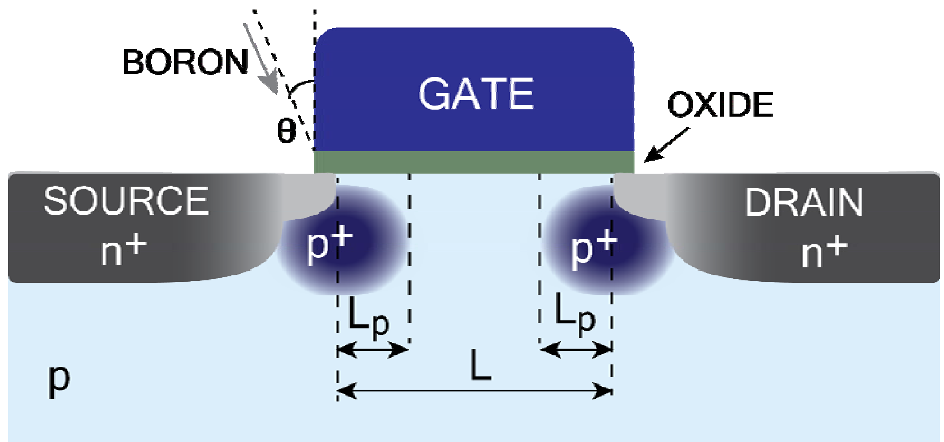
where N_t^* is the so-called apparent trap density given by $N_t(E_{\text{fn}})(1 \pm \alpha\mu N)^2$

N_t^* is approximated by the following function of N:

$$N_t^*(E_{\text{fn}}) = A + BN + CN^2$$

Halo (Pocket) Implant

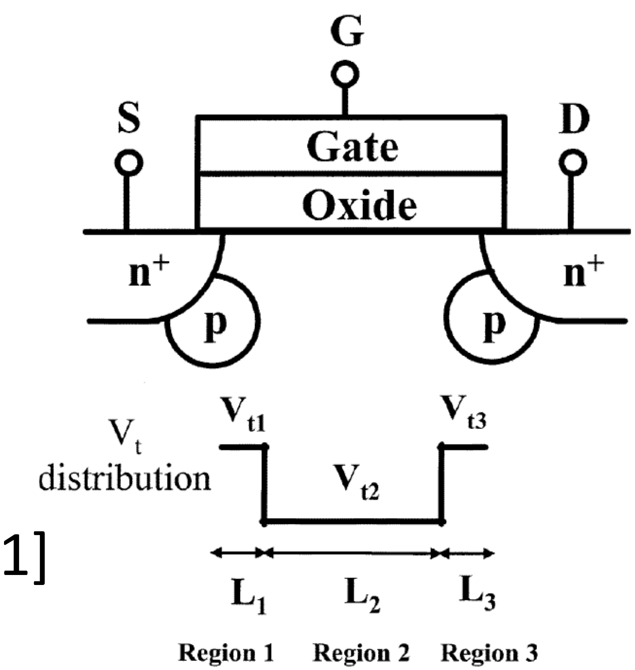
- non-uniform doping concentration



Approaches Suggested in Literature

Assuming only non-uniform doping concentration:

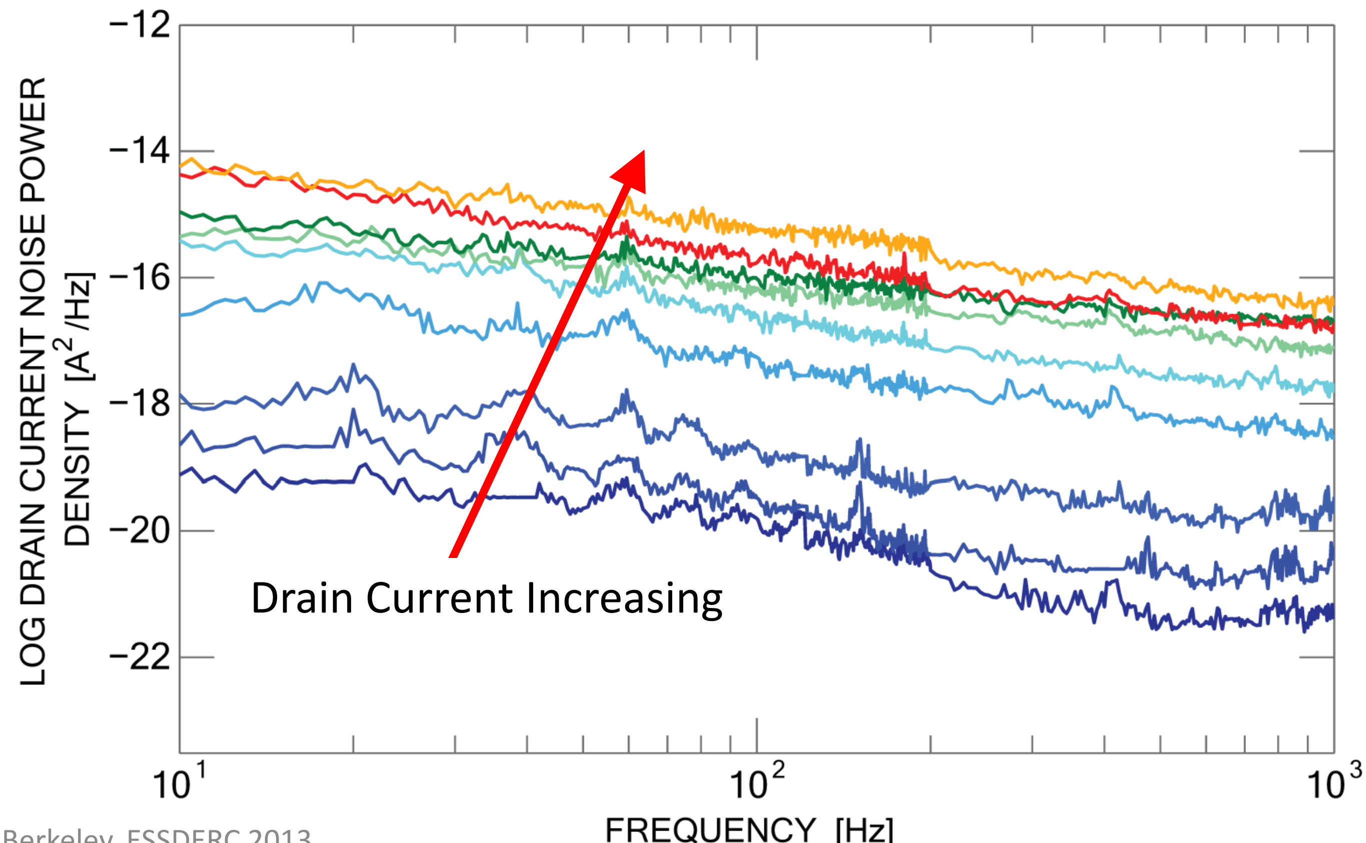
$$
\begin{aligned}
\frac{S_{\mathrm{id}}}{I_d^2} &= \frac{kT}{\gamma f W L_{\mathrm{eff}}^2} N_t(E_{\mathrm{fn}}) \\
&\quad \times \left[\int_{L_1} \frac{1}{N_1^2(x)} dx + \int_{L_2} \frac{1}{N_2^2(x)} dx + \int_{L_3} \frac{1}{N_3^2(x)} dx \right] \\
&\approx \frac{kTq^2}{\gamma f W L_{\mathrm{eff}}^2 C_{\mathrm{ox}}^2} N_t(E_{\mathrm{fn}}) \\
&\quad \times \left[\frac{L_1}{(V_g - V_{t1})^2} + \frac{L_2}{(V_g - V_{t2})^2} + \frac{L_3}{(V_g - V_{t3})^2} \right]
\end{aligned}
$$
[11]



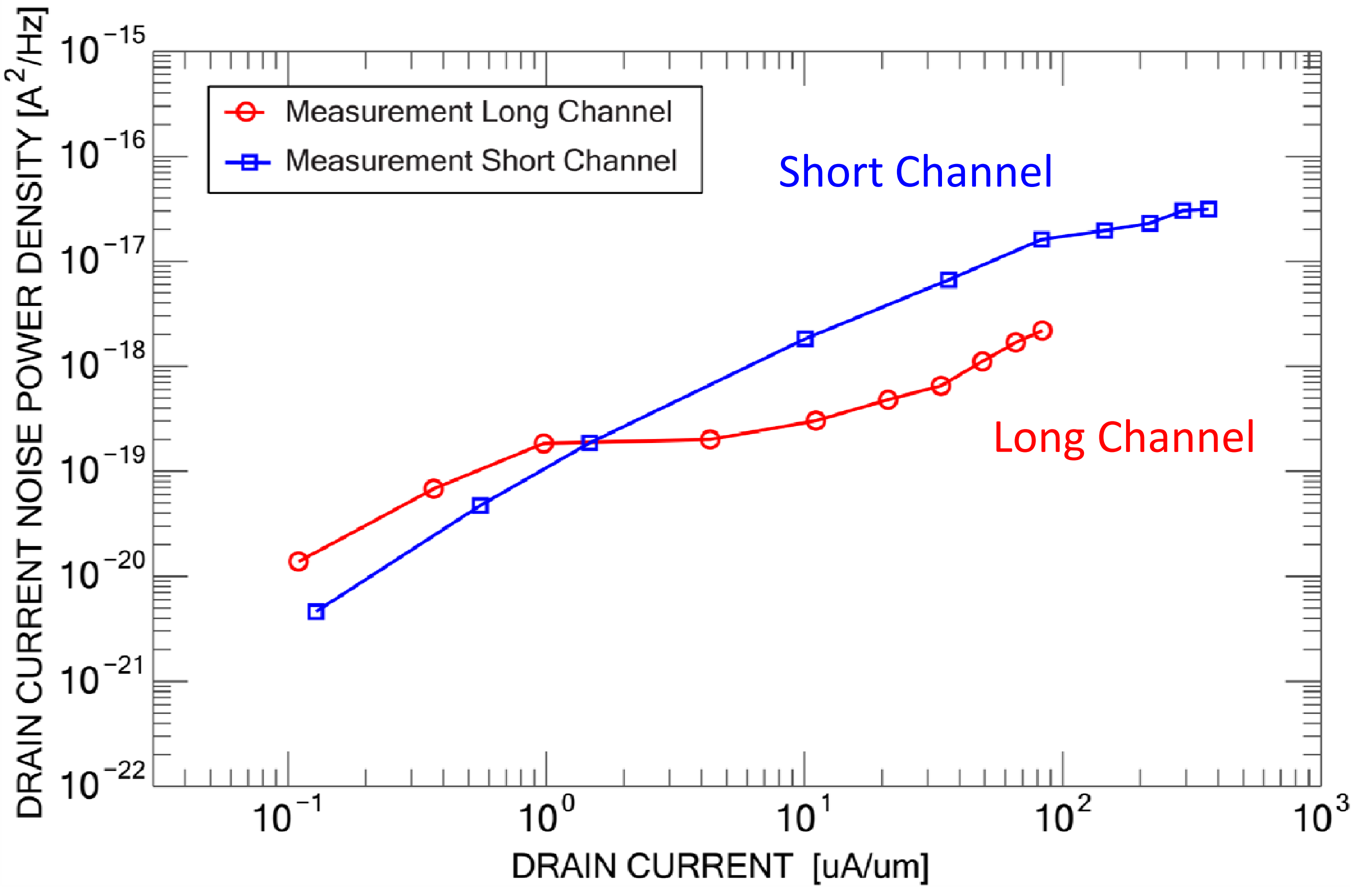
The equation and the graph have been taken directly from [11]:
Pocket implantation effect on drain current flicker noise in analog nMOSFET devices, Wu *et al.*, TED, vol. 51, no. 8, 2004

Measurement

- Measurements were done on short and long-channel NMOSs fabricated by CMOS 45-nm node technology
- A S300 semi-auto prober with BTA9812 noise analyzer were used



Measurement

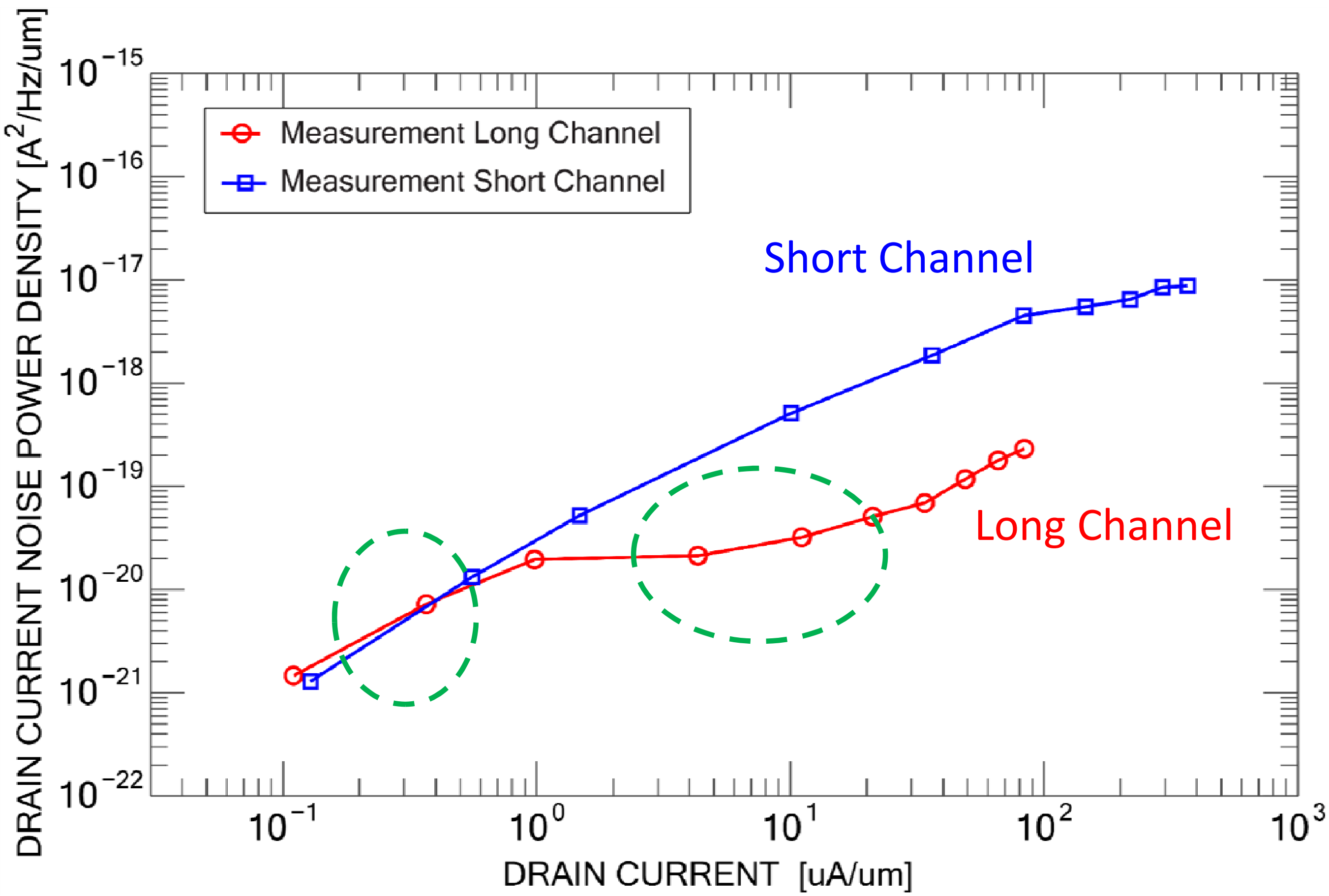


Width:

Long-channel: 10 µm

Short-channel: 5 µm

Measurement

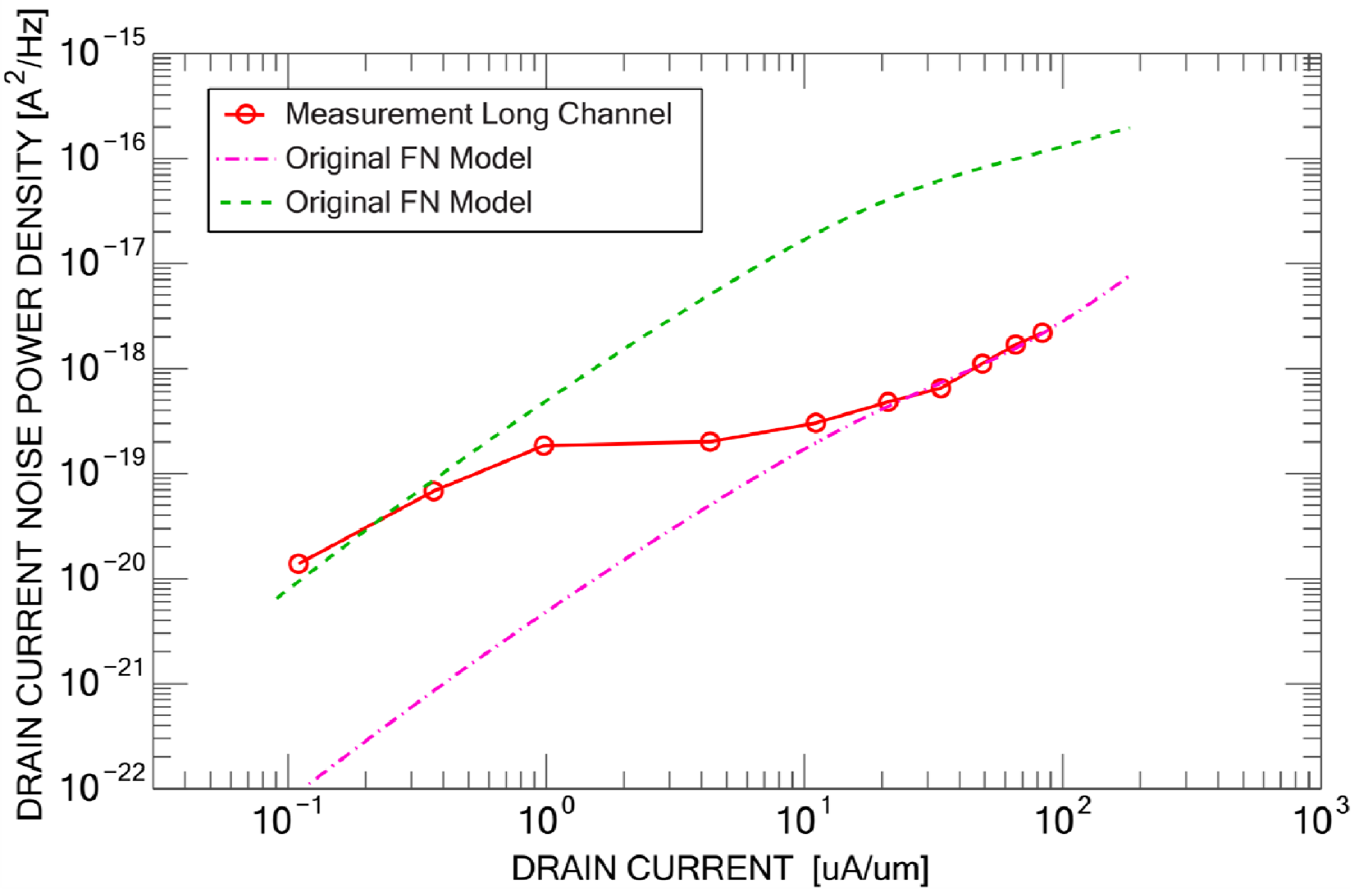


Observations:

1) Comparable Noise in Short and long channels

2) Significant bias dependence

Measurement



Observations:

1) Comparable Noise in Short and long channels

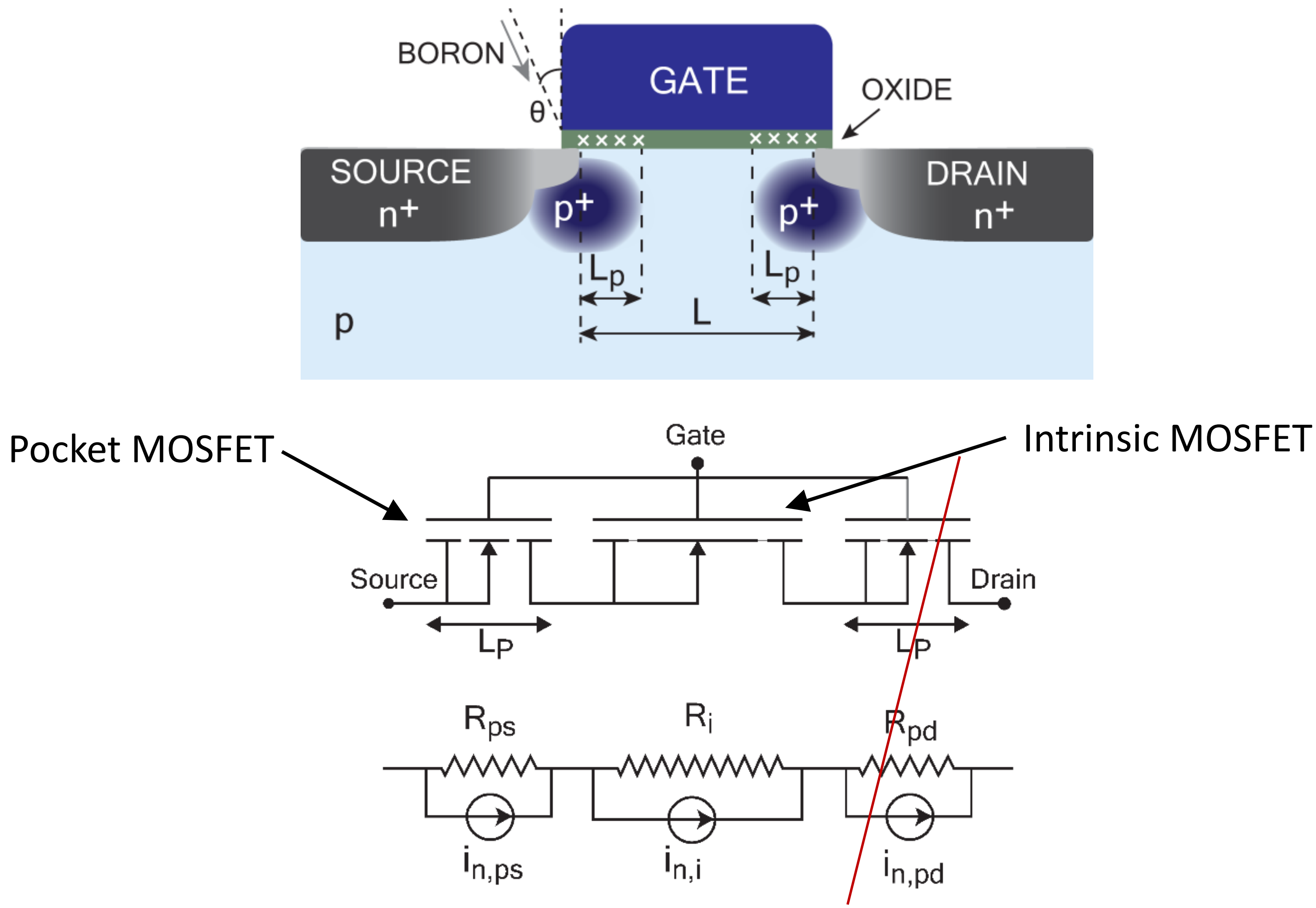
2) Significant bias dependence

3) Usual practice of the unified flicker-noise model is inadequate

⇩

More complex mechanisms are Involved.

Methodology



Methodology cont.

- Weighted contributions based on the equivalent transimpedances

$$S_{\mathrm{ID}}(f) = \boxed{\frac{{R_p}^2}{(R_p + R_i)^2} S_{\mathrm{ID,p}}(f) + \frac{{R_i}^2}{(R_p + R_i)^2} S_{\mathrm{ID,i}}(f)}$$

HSPICE,
small signal analysis

BSIM6

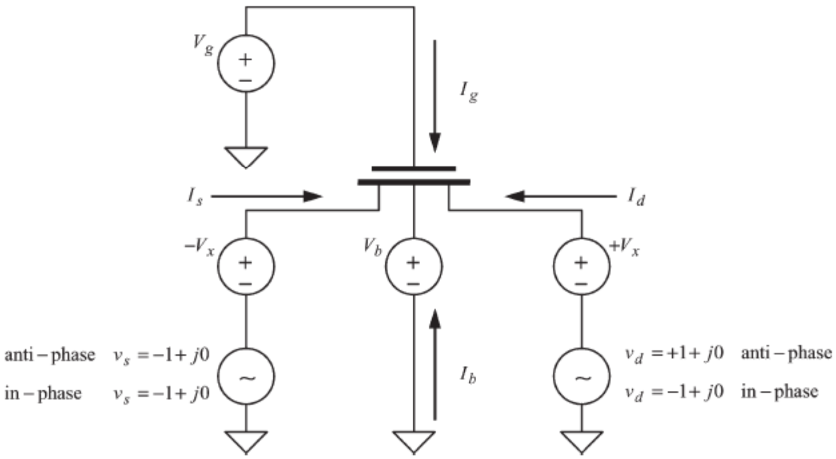
BSIM6: Industry Standard bulk model

- BSIM6 – Industry standard bulk MOSFET model
  - All real device effects (SCE, CLM etc.) from BSIM4
- Symmetry
  - Currents, Caps & derivatives are symmetric @ VDS=0
  - Provide accurate results in analog/RF simulations e.g. Harmonic Distortion simulation
- Physical Capacitance model
- Smooth behavior in all regions of operations
  - Faster Convergence

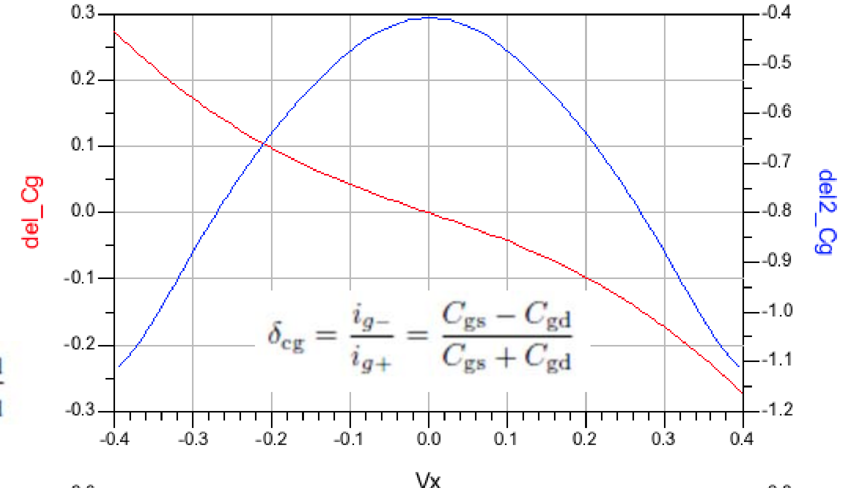
BSIM6: AC Symmetry test

(C. McAndrew, IEEE TED, 2006)

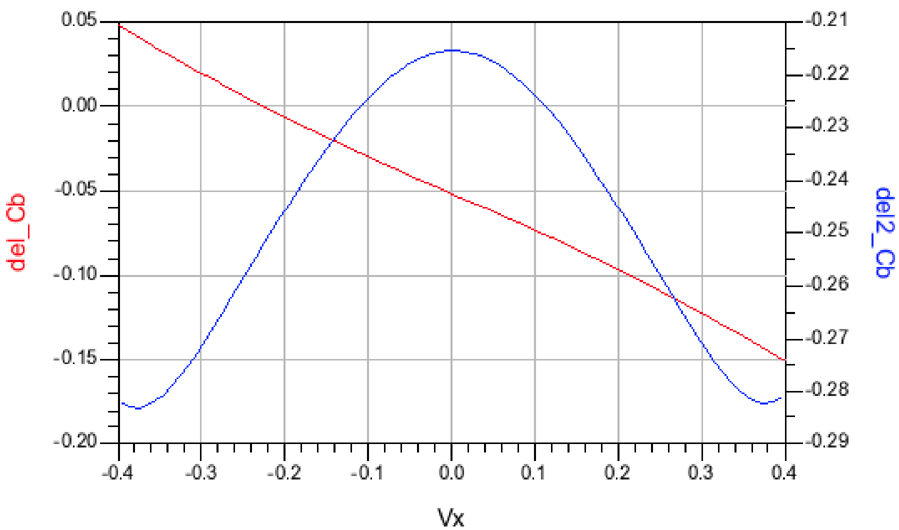
Capacitance & derivatives are symmetric

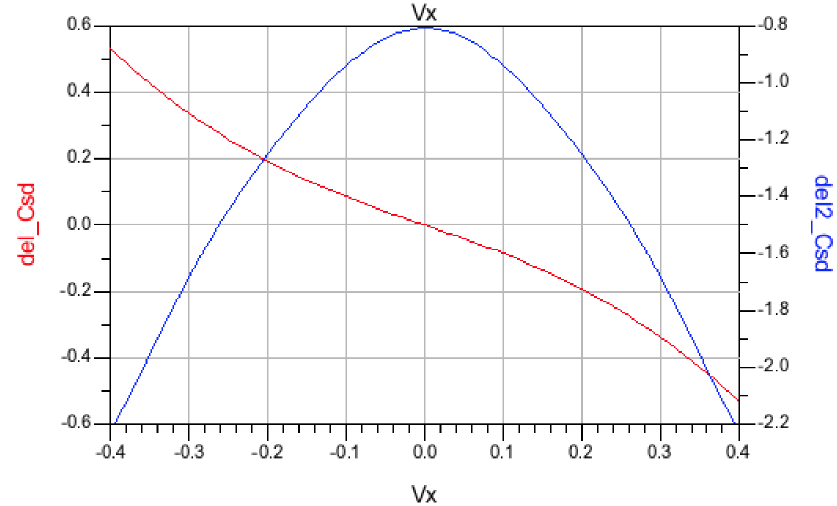


$$\delta_{\mathrm{csd}} = \frac{(i_{s-} + i_{d-}) + (i_{s+} - i_{d+})}{(i_{s-} - i_{d-}) + (i_{s+} + i_{d+})} = \frac{C_{\mathrm{ss}} - C_{\mathrm{dd}}}{C_{\mathrm{ss}} + C_{\mathrm{dd}}}$$

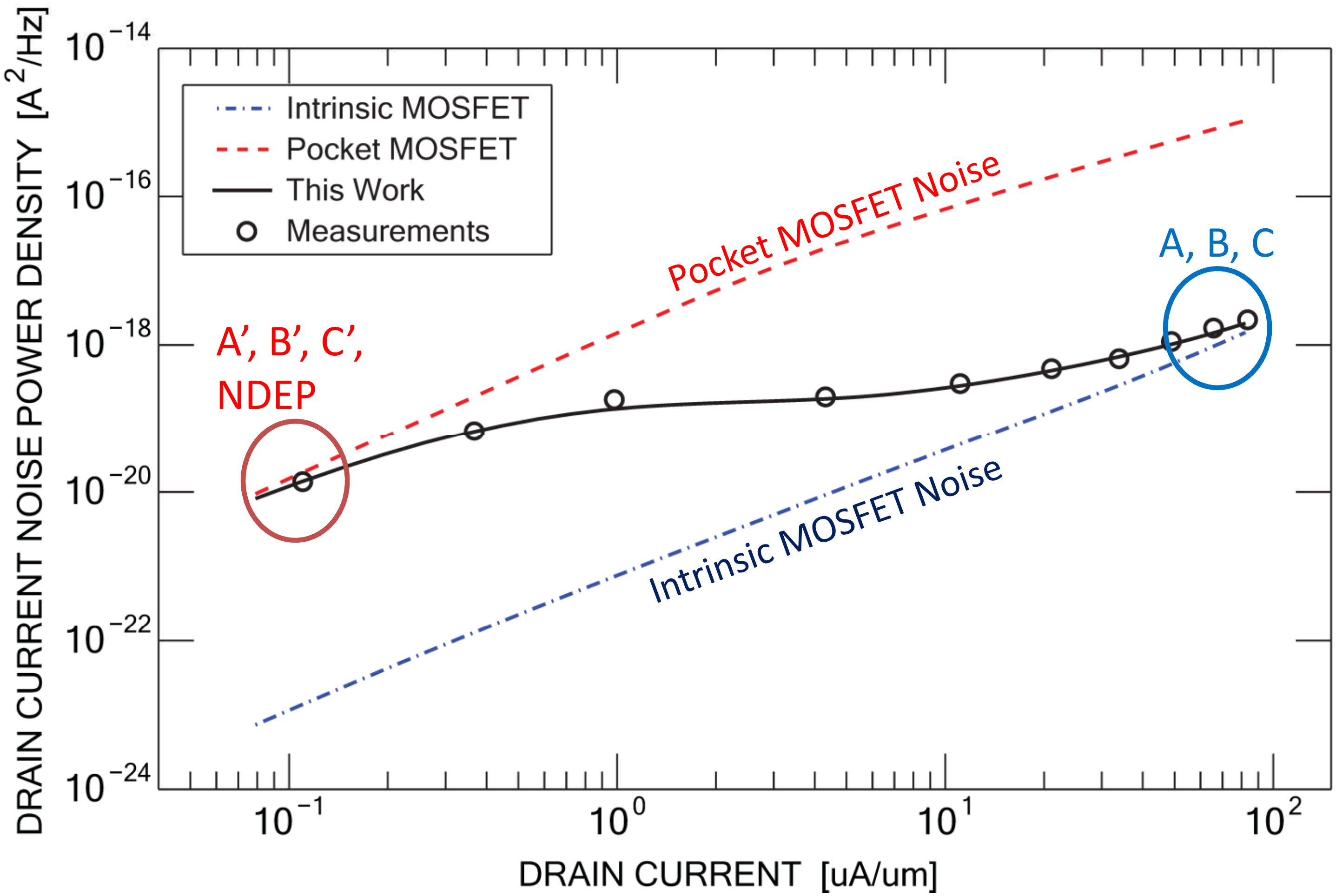


$$\delta_{\mathrm{cg}} = \frac{i_{g-}}{i_{g+}} = \frac{C_{\mathrm{gs}} - C_{\mathrm{gd}}}{C_{\mathrm{gs}} + C_{\mathrm{gd}}}$$





Model Validation: Long Channel



Discussion

$$R = \frac{1}{qn\mu} \times \frac{L}{S}$$

Subthreshold

1. For an applied V_g, pocket MOSFET will have smaller surface potential
2. The carrier's number depends exponentially on the surface potential
3. Pocket MOSFET will show a much higher channel resistivity
4. $R_p \gg R_i$
5. $S_{\mathrm{ID}}(f) = \cancelto{1}{\frac{{R_p}^2}{(R_p+R_i)^2}} S_{\mathrm{ID,p}}(f) + \cancelto{0}{\frac{{R_i}^2}{(R_p+R_i)^2}} S_{\mathrm{ID,i}}(f) \approx S_{\mathrm{ID,p}}$

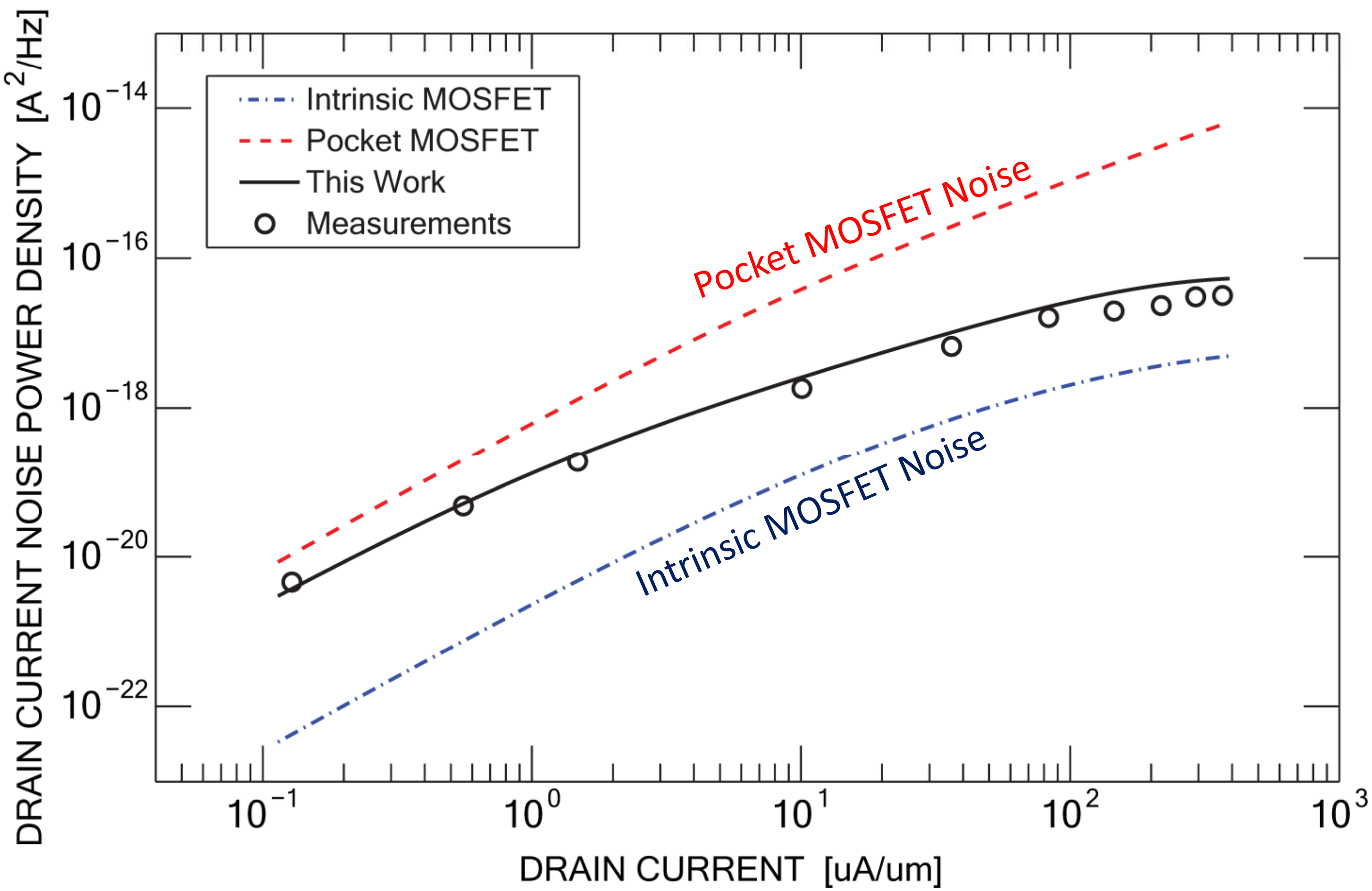
Discussion

$$R = \frac{1}{qn\mu} \times \frac{L}{S}$$

Strong Inversion

1. The resistivity of both channels drops dramatically
2. The resistance of the segments will be distinguished by their lengths
3. $R_i \gg R_p$
4. $S_{\mathrm{ID}}(f) = \cancelto{0}{\frac{{R_p}^2}{(R_p+R_i)^2}} S_{\mathrm{ID,p}}(f) + \cancelto{1}{\frac{{R_i}^2}{(R_p+R_i)^2}} S_{\mathrm{ID,i}}(f) \approx S_{\mathrm{ID,i}}$

Model Validation: Short Channel



Discussion

- **Subthreshold**

$$S_{\mathrm{ID}} \approx S_{\mathrm{ID,p}}$$

- **Strong Inversion**

  The length of the pocket and the length of the intact channel is comparable => a smoother and shallower transition

$$S_{\mathrm{ID,i}} < S_{\mathrm{ID}} < S_{\mathrm{ID,p}}$$

- In a case of a very short channel MOSFET, the pockets from the two sides merge => conventional shape of the transition from subthreshold to strong inversion is restored

Discussion

Unified Flicker Noise Model:

- Step 1) The noise power density of the local current fluctuations $S_{\Delta\mathrm{Id}}$ is calculated.

- Step 2) The contributions of the local noise sources to the fluctuation of the output current are combined:

$$S_{\mathrm{ID}}(f) = \frac{1}{L^2}\int_0^L S_{\Delta\mathrm{Id}}(x,f)\Delta x dx$$

Conclusions

- The usual practice of the unified flicker-noise model is inadequate for MOSFETs with pocket implants, BSIM4, PSP, …

- Of particular interest for *near-threshold RF design*:

  The non-uniform bias-dependent impedance distribution causes the subthreshold FN power density to be dominated by the contribution from the source-side pocket

- The proposed model is the **only** method so far that can predict FN power density as a function of the device geometry and across different bias regimes.

THANKS FOR LISTENING, ANY QUESTION?