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Scalability of UTBB InGaAs MOSFETs on Silicon

Extending the FDSOI roadmap…

III-V CMOS for advanced nodes

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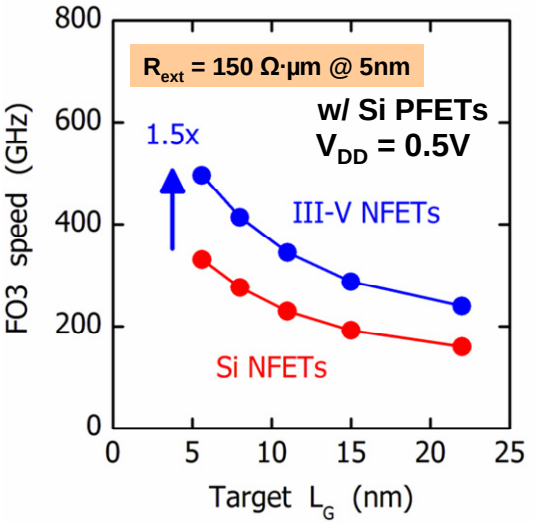
Motivation – Power reduction and Diversification

- **Reduce the power consumption of advanced CMOS nodes by scaling V_{DD} to 0.5V**
  - Introduce III-V materials as channel material for n-MOSFETs

➔ Up to 1.5x switching speed improvement including parasitics

  - Corresponds to 2 to 3 generations improvement



- **New trends in the mobile era – Smarter planet**
  - Smarter cities – smarter grids – personalized health care
  - Small, integrated communicating nodes ➔ **III-V RF**
  - Big data → Data transfer becomes the bottleneck
  - ➔ **III-V lasers for on-chip optical interconnects**

➔ III-V on Si is a versatile technology platform for diversification – integration of new functions

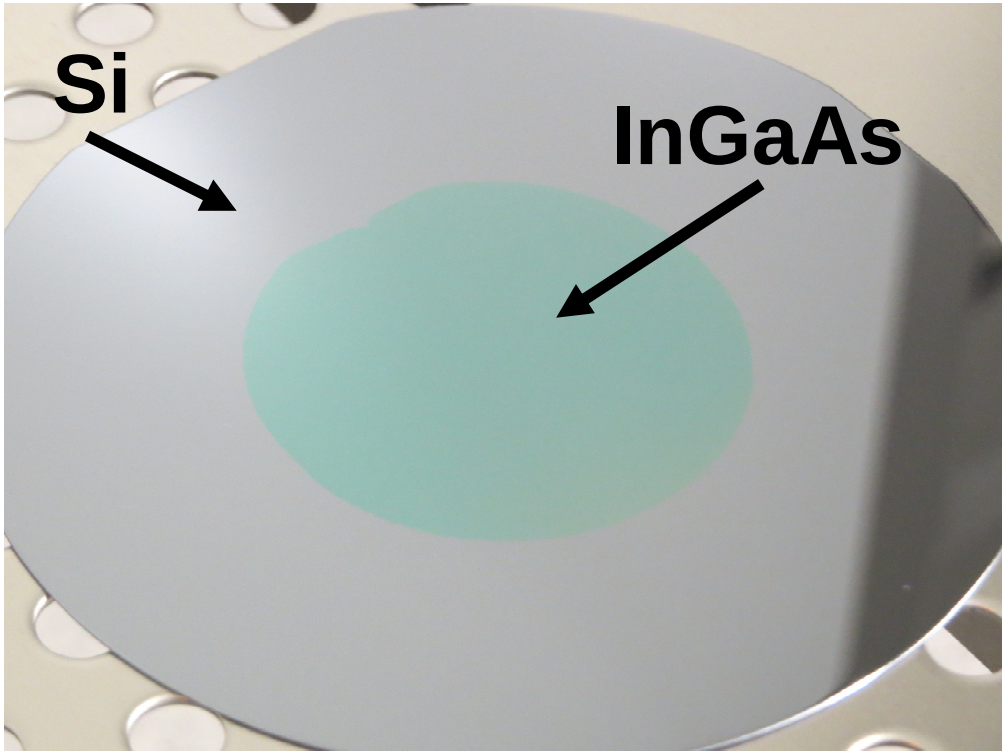
Welcome to the Decade of Smart

Outline

- **Substrates: InGaAs-on-insulator platform**
- **Devices: Scaling (emphasis on DIBL)**
- **Simulations: smaller gate lengths…**

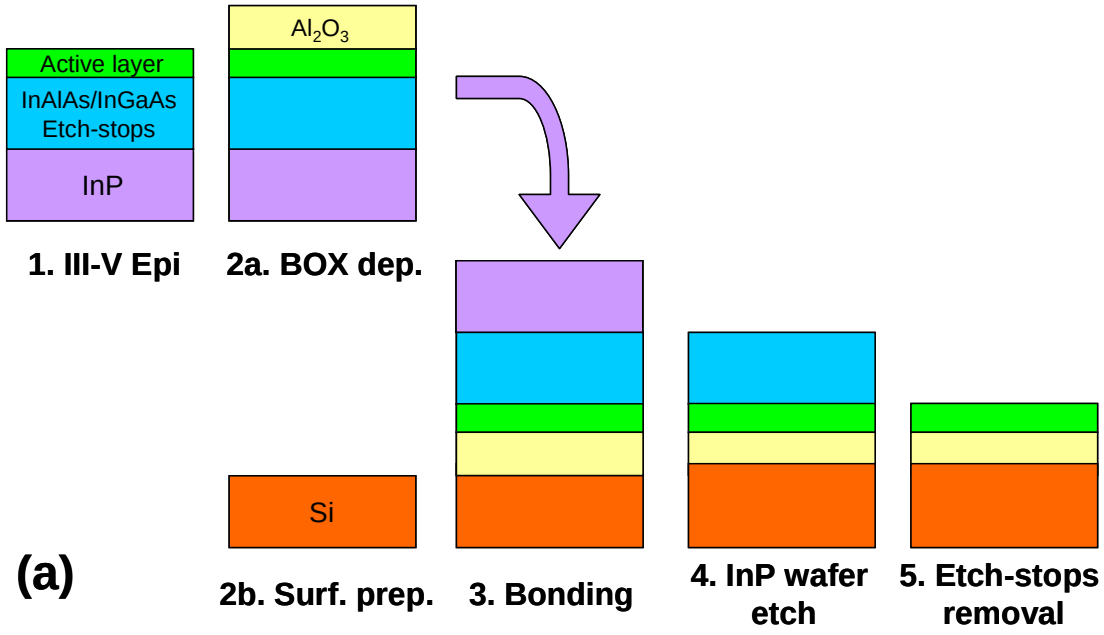
Substrate – The SOI-like solution

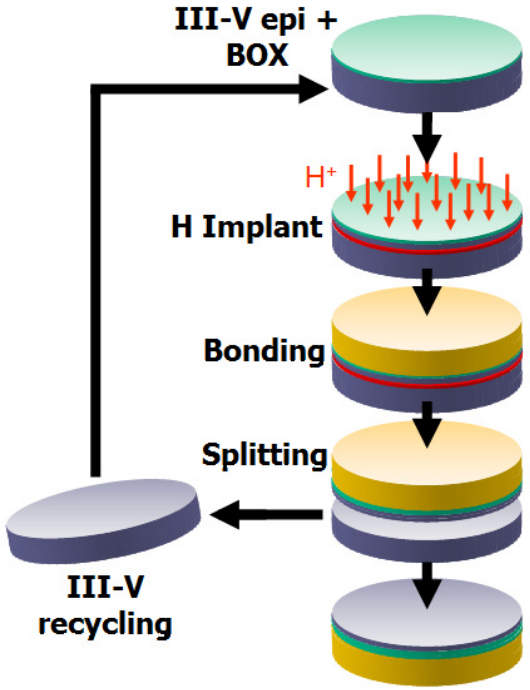
- **InGaAs-on-insulator by direct wafer bonding as a platform**
  - III-V integration on Silicon substrates / co-integration with Si/SiGe devices
  - Device scalability: base for advanced FDSOI/FinFETs architectures



Substrate – Fabrication

- **InGaAs-on-insulator by direct wafer bonding**
  - UTBB Targets: **6 nm InGaAs and 10 nm BOX** on Si
  - Two possible methods: with or without recycling the donor wafer

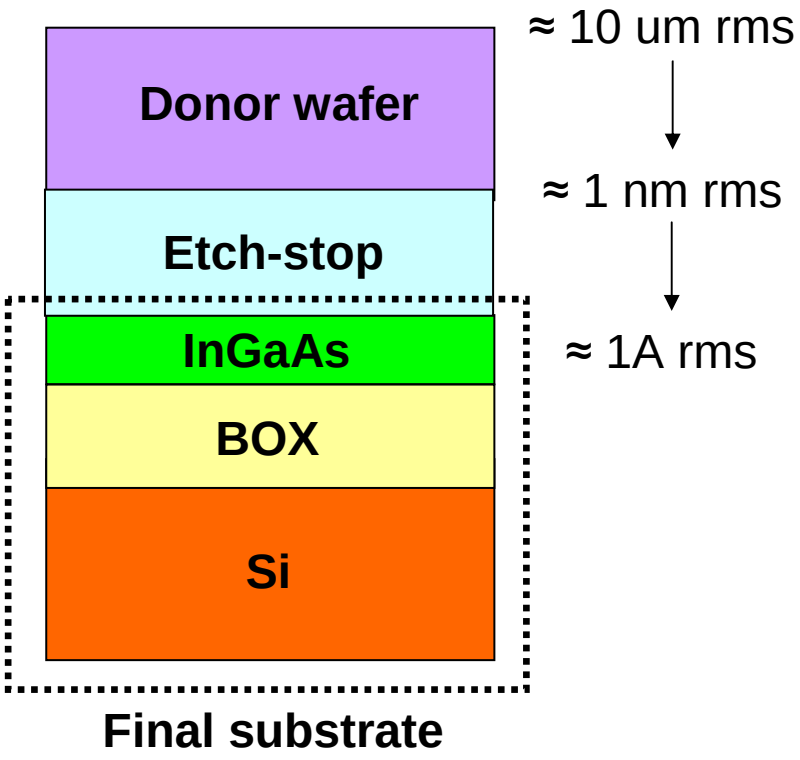


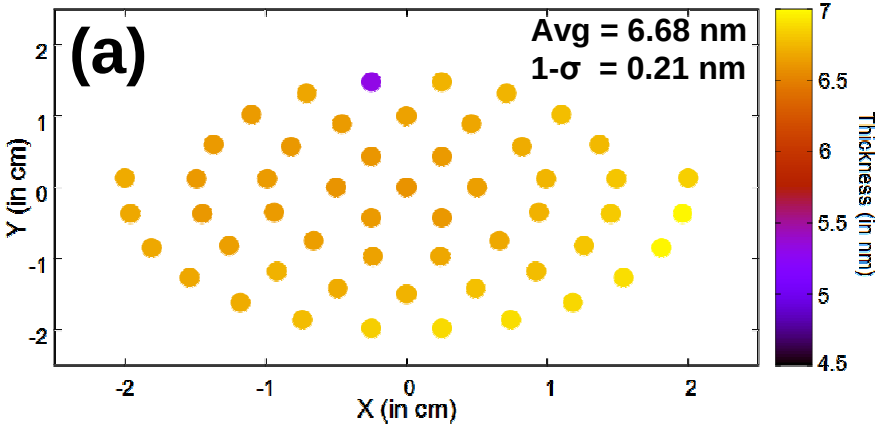


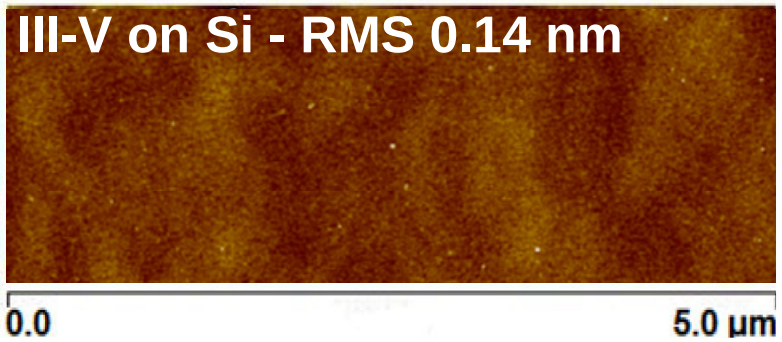
L. Czornomaz, et al., IEDM (2012)

Substrate – Thickness, homogeneity, roughness

- **Excellent parameters control compared to SOI fabrication**
  - Key process steps are no longer implantation / CMP / oxidation-etch
  - Thickness, homogeneity, composition and roughness: defined by the III-V growth step





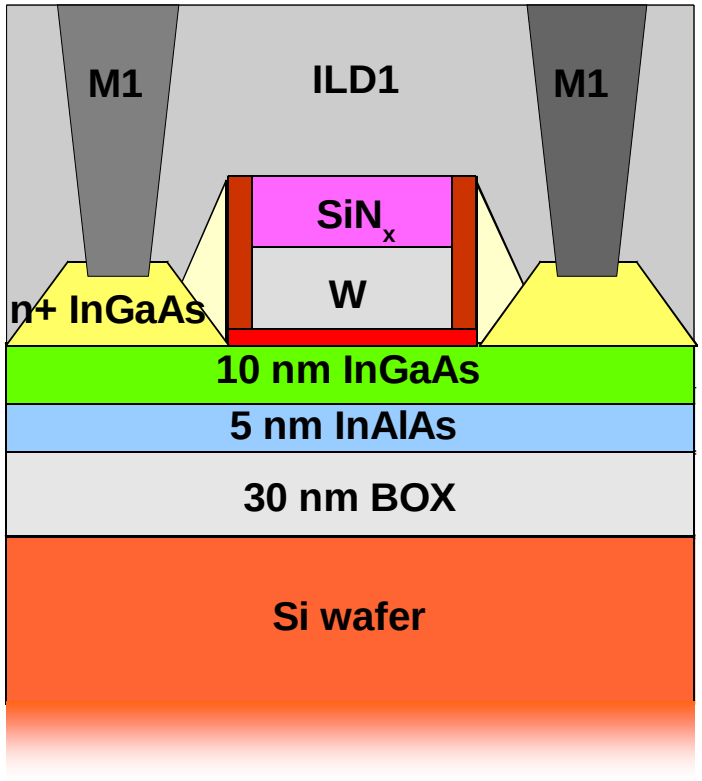


Outline

- **Substrates: InGaAs-on-insulator platform**
- **Devices: Scaling (emphasis on DIBL)**
- **Simulations: smaller gate lengths…**

Devices – Process flow

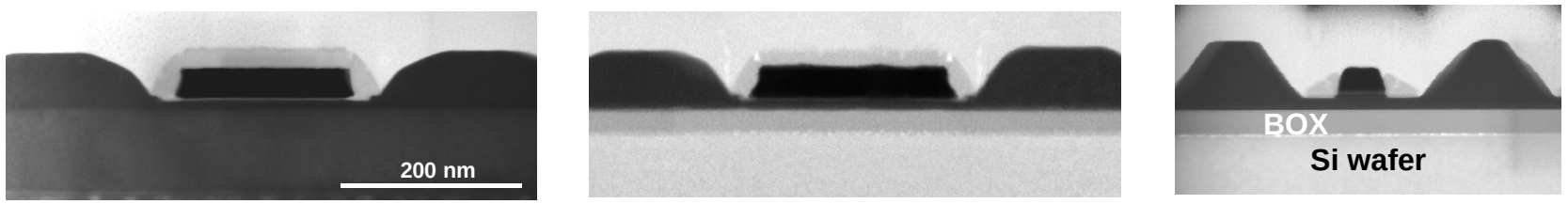
- **Self-aligned CMOS-like InGaAs MOSFETs**
  - **10 nm InGaAs** / 5 nm InAlAs on **30 nm BOX** on Si
  - Gate-first (**18A EOT**), implant-free raised source/drain

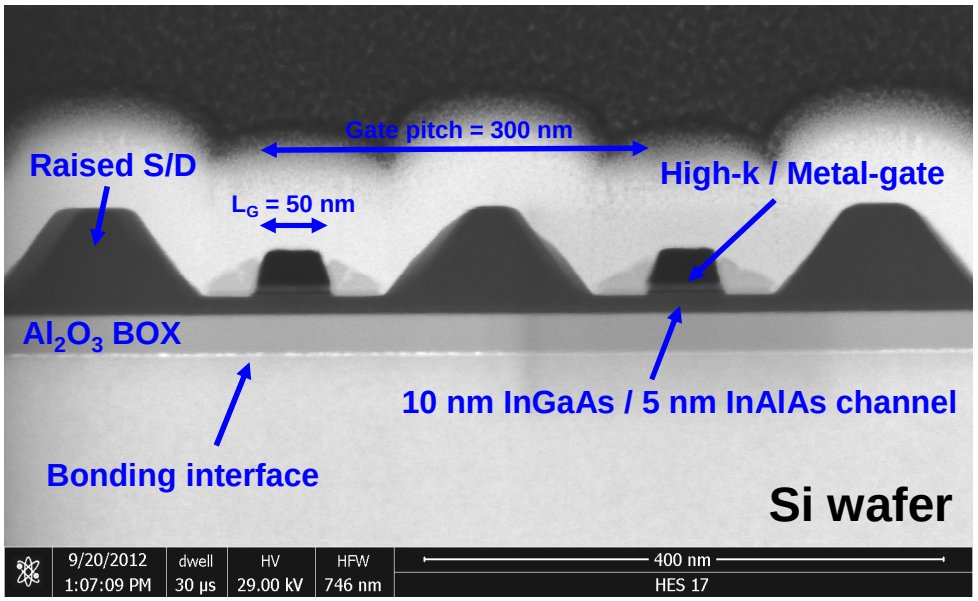


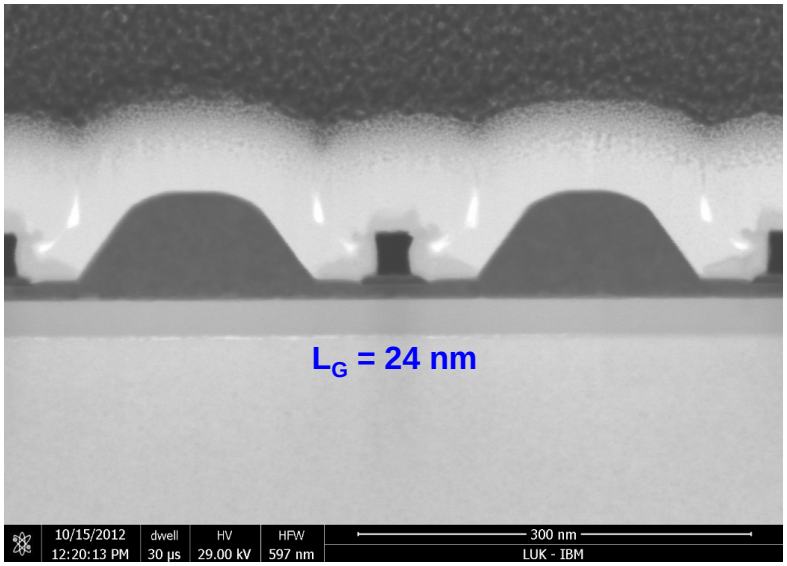
- **UTBB InGaAs on Si substrate fabrication**
- **Mesa isolation**
- **High-k / Metal gate / Gate cap deposition**
- **E-beam exposure and gate patterning**
- **Sidewall spacers formation**
- **In-situ doped InGaAs S/D regrowth (600ºC)**
- **ILD1 deposition and patterning**
- **M1 contacts**

Devices – From bulk to on-insulator substrates

Long channel on InP (DRC 2012) → **Long channel on Si (IEDM 2012)** → **Short channel on Si (ESSDERC 2013)**



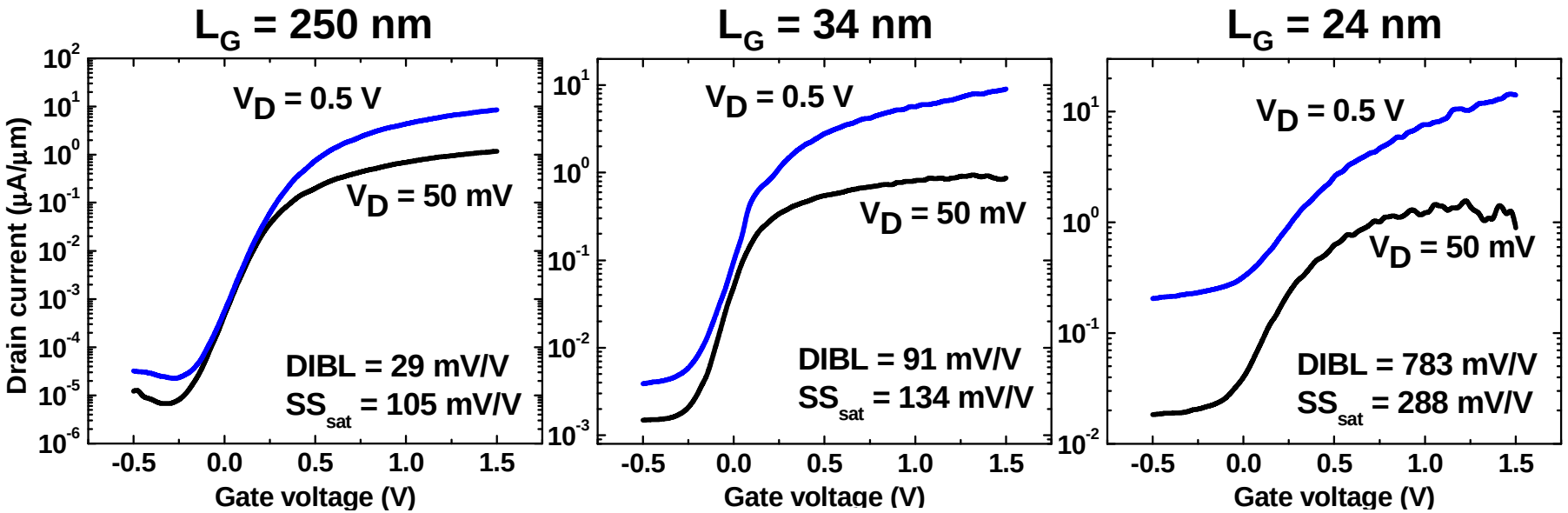




- **InGaAs-OI FETs successfully fabricated at 300 nm pitch and 24 nm gates**

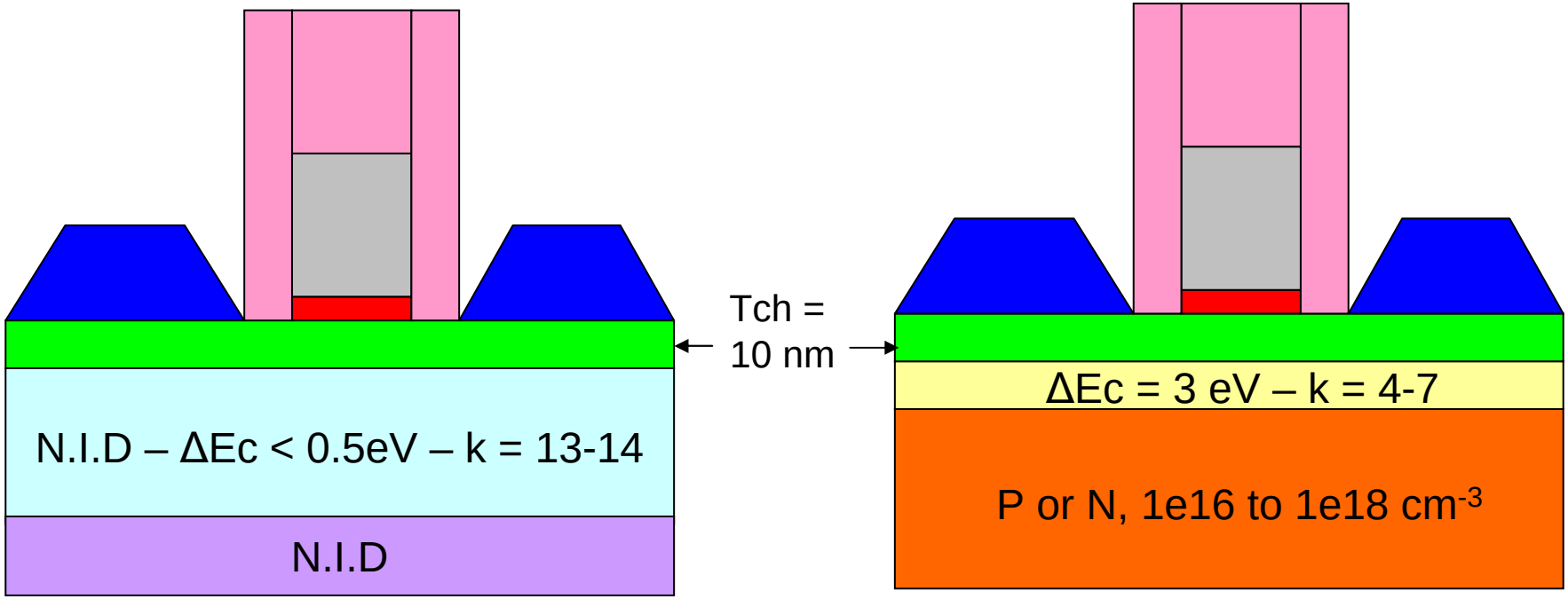
Devices – Transfer characteristics

- Well behaved FET operation down to 34 nm ($I_{ON}/I_{OFF} > 10^3$)
- Severe Short-channel effects at 24 nm → Tch = 10 nm needs to be scaled
- Low I_{ON} due to large access resistance



Devices – Electrostatic integrity

- **Comparing "bulk" and "UTBB" architectures <u>with thin channels</u>**

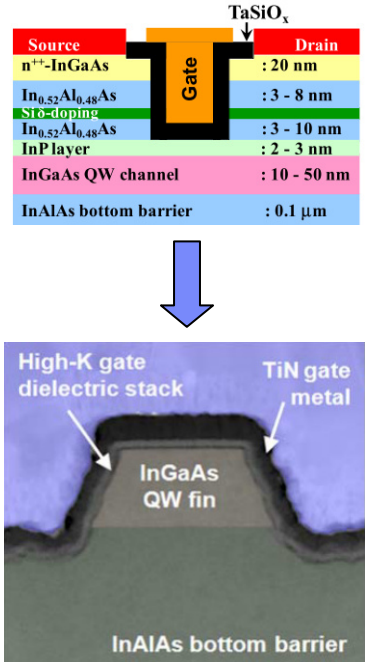


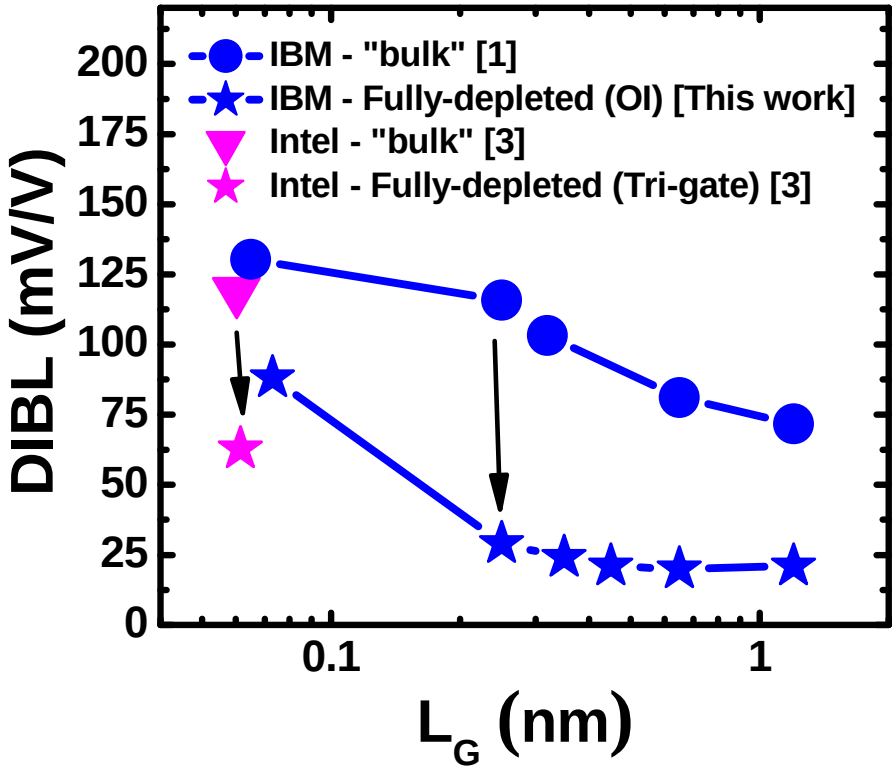
- **Real "SOI-like" structure ? NO !**
  - High dielectric constant → Large E-fields
  - Low doping → Large S/D depletion regions
  - Low band offset → no ground plane

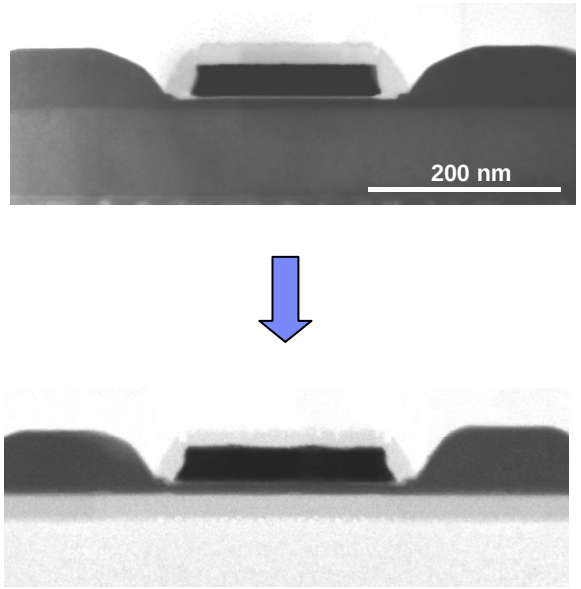
DIBL scalability should be very different

Devices – Electrostatic integrity

- **Comparing "bulk" and "UTBB" architectures with thin channels**



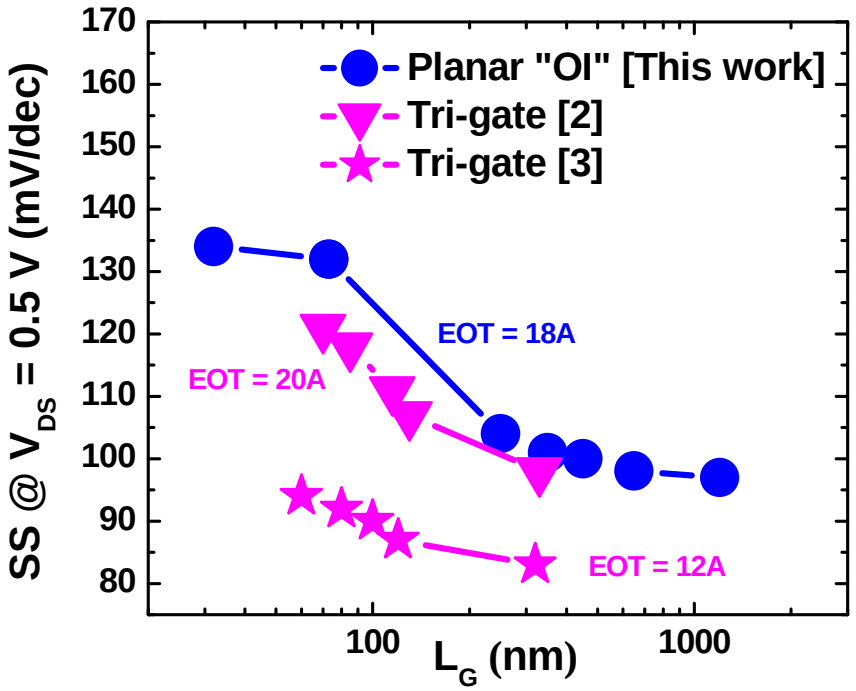


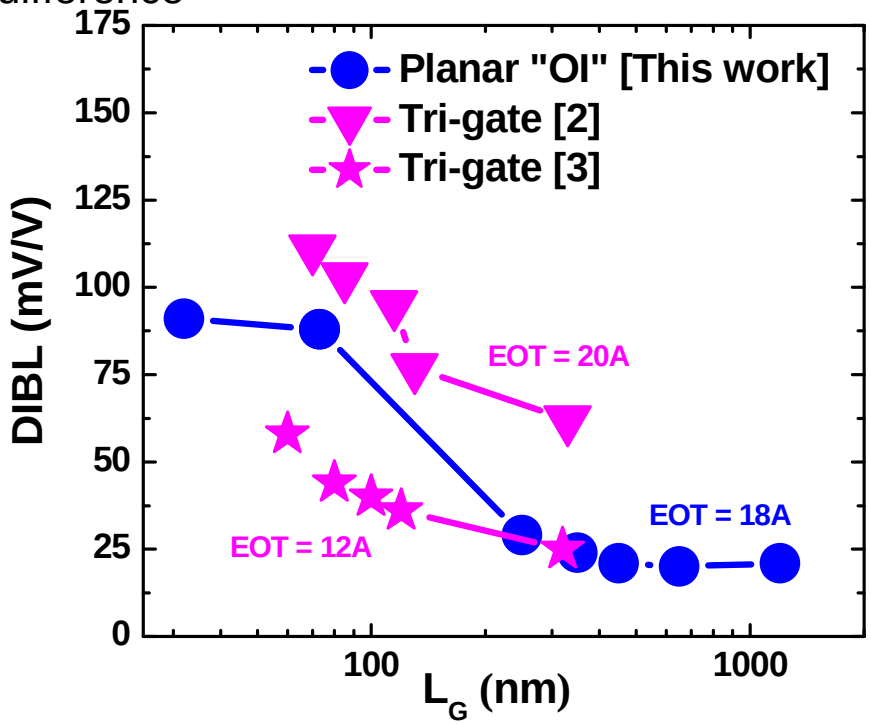


[1] L. Czornomaz, et al., DRC (2012)
[3] M. Radosavljevic, et al., IEDM (2011)

Devices – Electrostatic benchmark to Tri-gate

- **Compare scaling in existing Planar-OI vs Tri-gate devices**
  - **10nm InGaAs** / 30nm BOX vs **30nm Fins**
  - SS is higher on planar → Dit is higher (different gate stack, thermal budget)
  - DIBL scaling is quite good given the EOT difference





[2] M. Radosavljevic, et al., IEDM (2010)
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Outline

- **Substrates: InGaAs-on-insulator platform**
- **Devices: Scaling (emphasis on DIBL)**
- **Simulations: smaller gate lengths…**

Simulations – Setup

Simu: P. Kerber – IBM T.J Watson

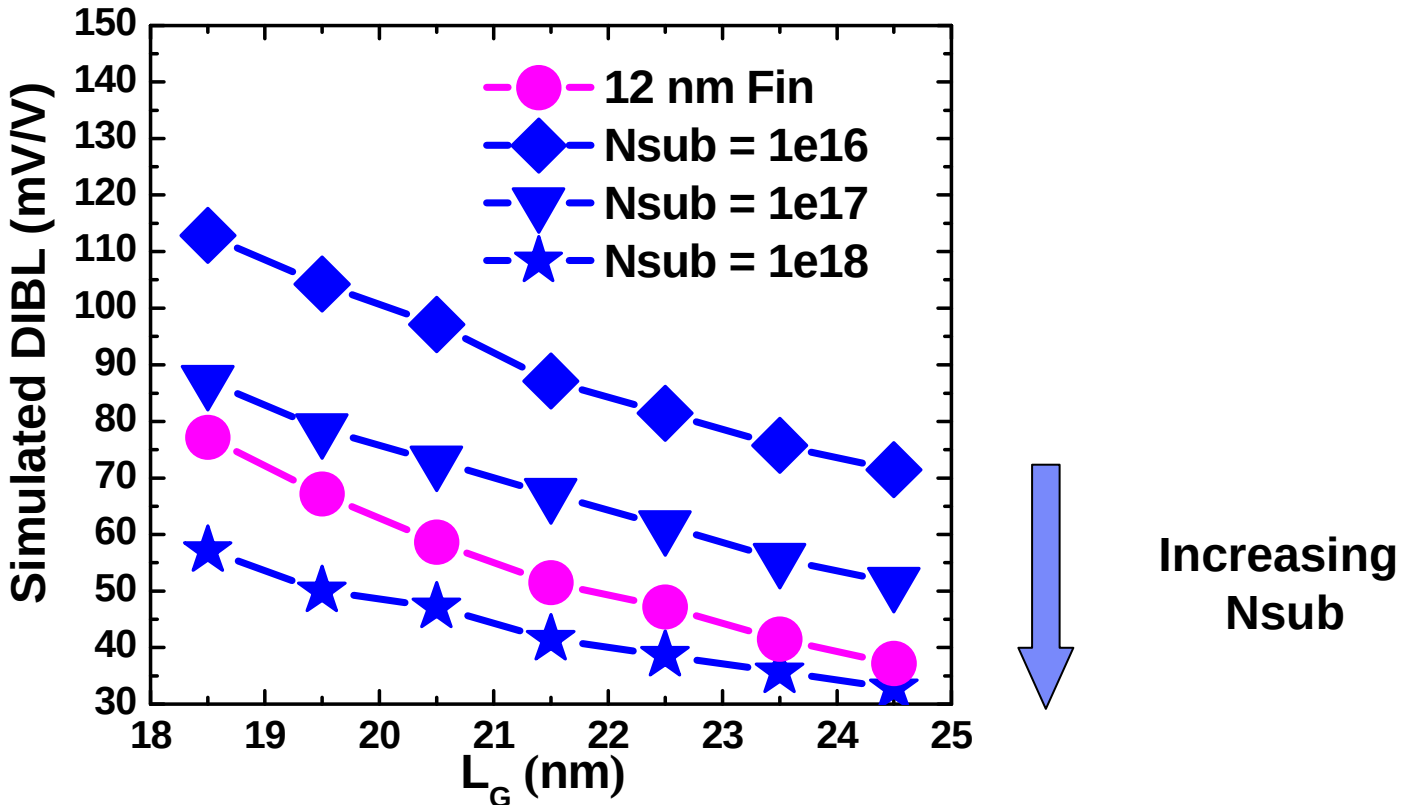
- **2D/3D simulations with FIELDAY (IBM)**
  - Models calibrated to **existing** MOSFETs data
  - Device parameters matched to **14 nm node** (Rext, EOT, doping profiles, …)
  - Drift-diffusion model with bandgap narrowing and Caughey-Thomas mobility models
  - No Dit and no quantization

- **What is the impact of substrate doping in UTBB InGaAs substrates ?**

- **What is the equivalence between fin width and planar channel thickness ?**

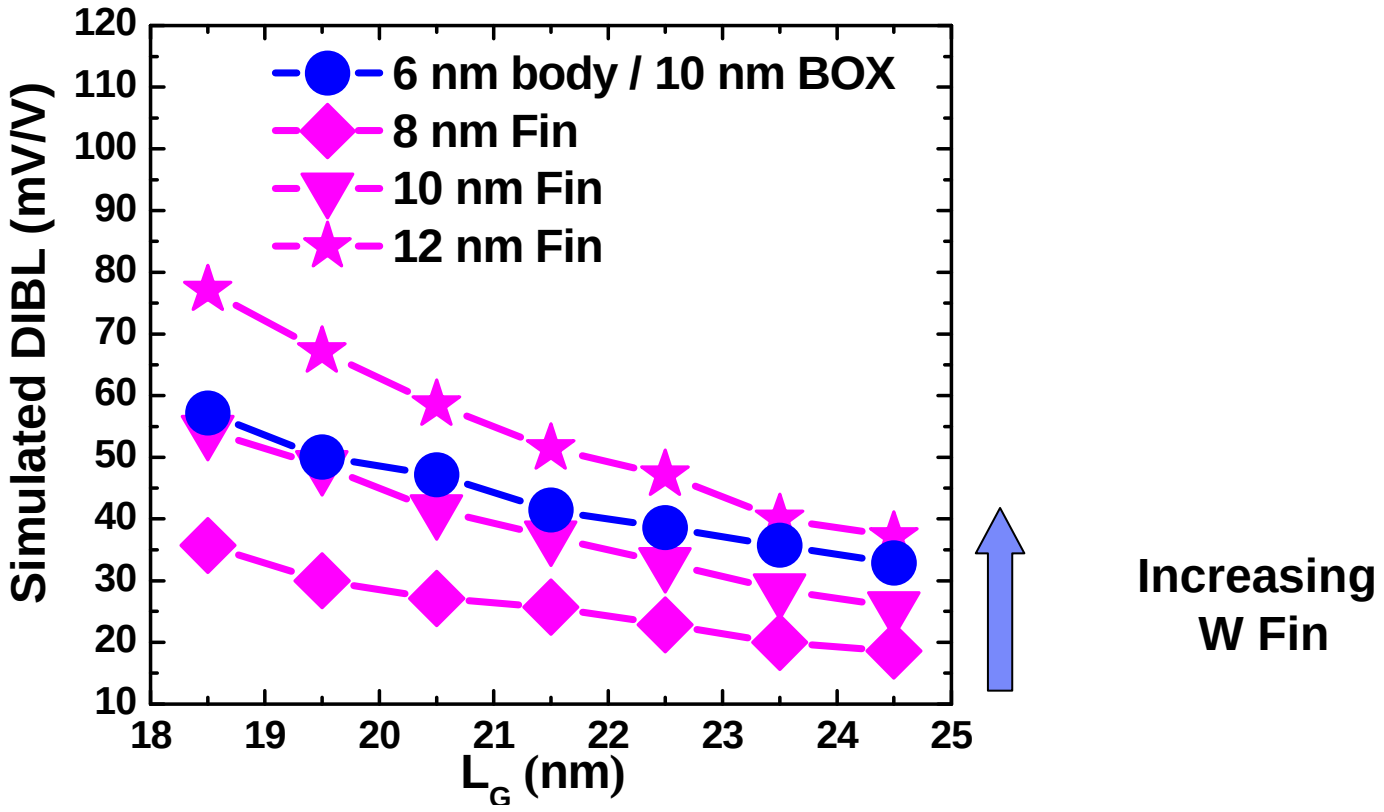
Simulations – Substrate doping (Ground plane)

- **What is the effect of substrate doping in UTBB InGaAs structures ?**
  - Comparing **6nm InGaAs / 10nm BOX** on Si vs **12nm InGaAs Fins**
  - Device parameters matched to 14 nm node (Rext, EOT, …)
  - No Dit, no quantization



Simulations – Planar vs Fins

- **Which Fin width is needed to match 6nm InGaAs / 10nm BOX perf. ?**
  - Device parameters matched to 14 nm node (Rext, EOT, …)
  - No Dit, no quantization



Summary

- **Excellent control of InGaAs-on-insulator key parameters thanks to heterostructures**
  - 6 nm InGaAs on 10 nm BOX on Si fabricated
- **Self-aligned CMOS-like process transferred from “bulk” to “OI” w/ 24 nm gates**
  - Competitive scalability compared to existing Tri-gate devices
- **Thin-channel on high-bandgap III-V is not similar to “OI” in terms of DIBL**
  - Clear benefit of “OI” thanks to the ground plane
- **High Si substrate doping improves SCE immunity in “OI” structures**
  - Improves the ground plane
- **UTBB InGaAs with 6 nm channel should be comparable to 10 nm fins**

Thank you

Acknowledgments

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