Performance Limit of Parallel Electric Field Tunnel FET and Improvement by Modified Gate and Channel Configurations

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Outline

Background

- Why tunnel FET (TFET)
- Parallel electric field TFET (PE-TFET)

Performance of PE-TFET

- Device fabrication
- Experimental results

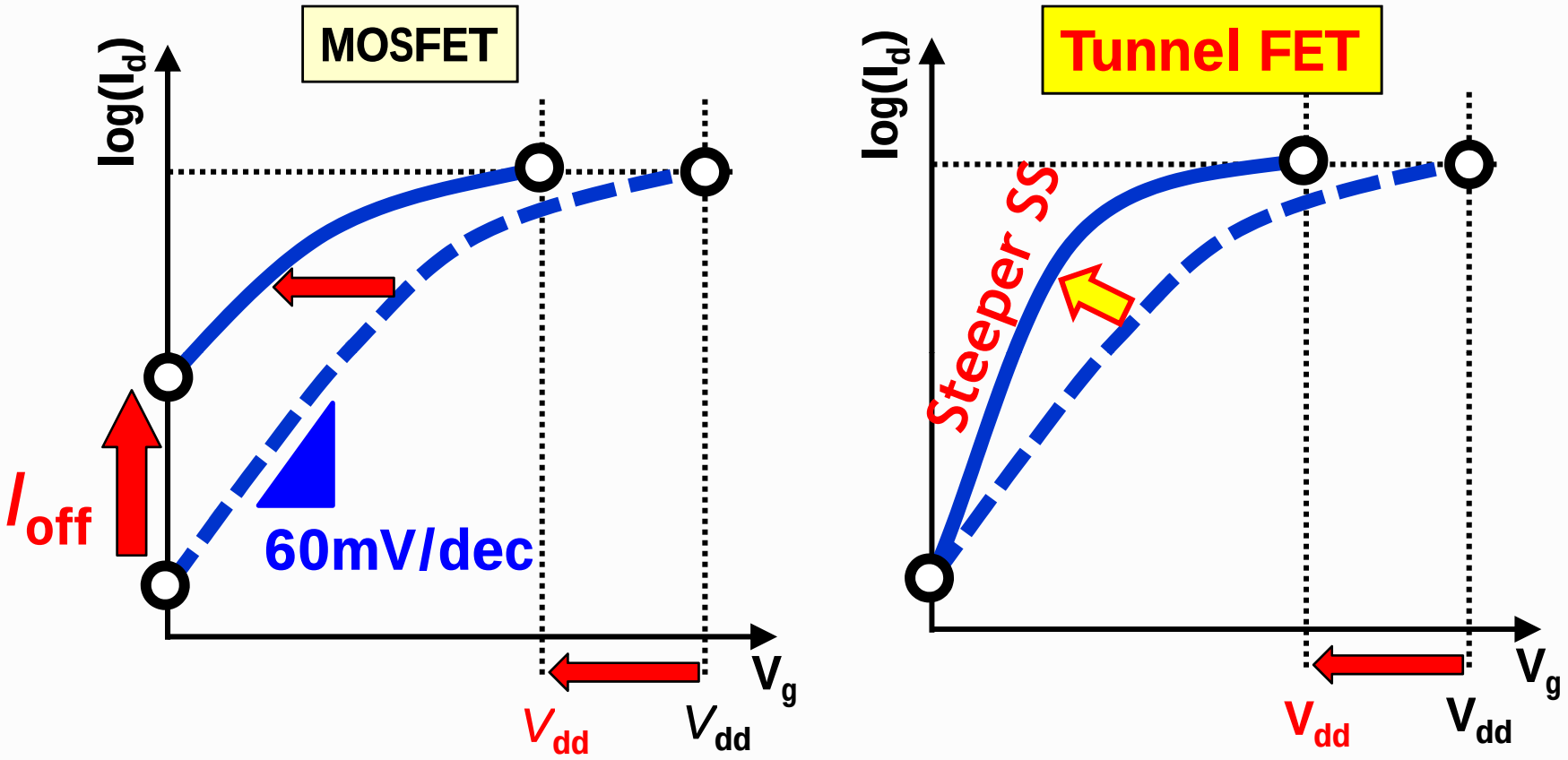
Proposal of Synthetic electric field TFET (SE-TFET)

- Device fabrication
- Experimental results

Summary

Why tunnel FET ?

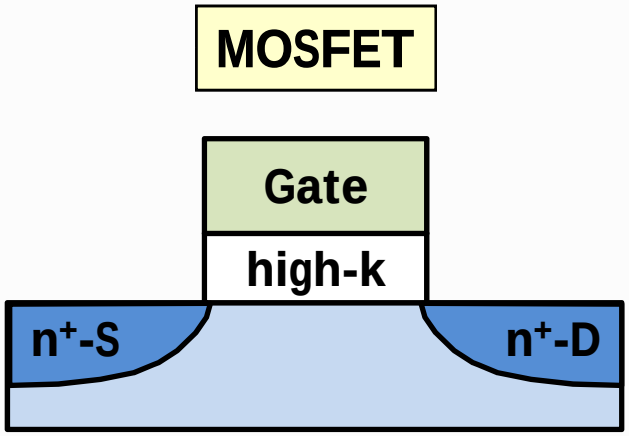
For V_{dd} Scaling

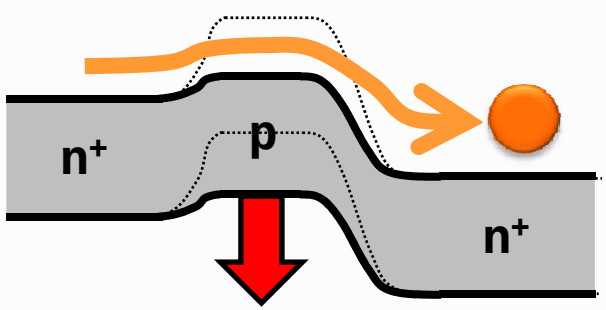


Conventionally V_{dd} scaling causes a significant increase in I_{off} due to the lower limit of SS (~60mV/dec.)

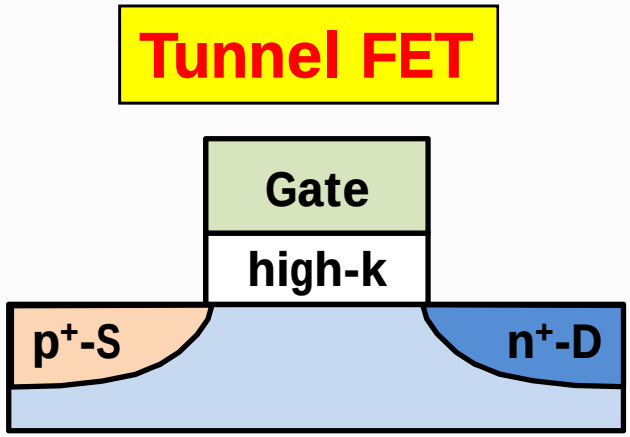
V_{dd} scaling without I_{off} increase can be done by *steepening the SS*

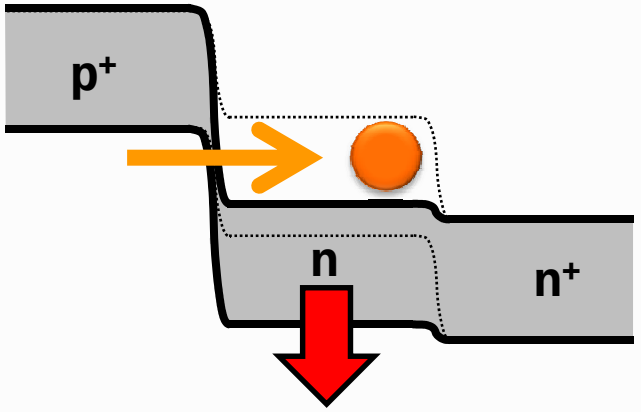
Why tunnel FET ?





Carrier flow is determined by thermal-injection mechanism
SS > 60mV/dec.



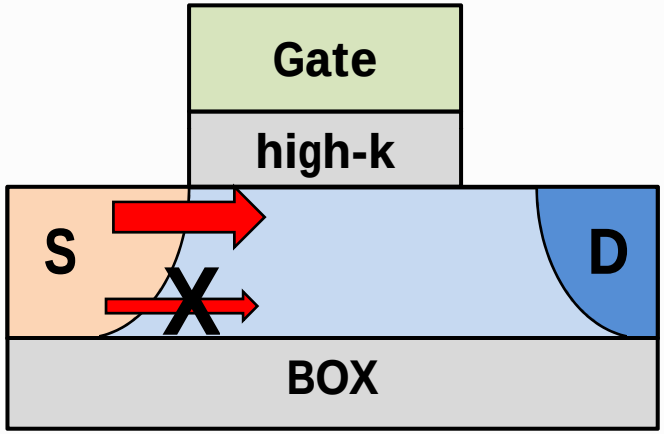


Carrier flow is determined by BTBT transport mechanism
SS < 60mV/dec.

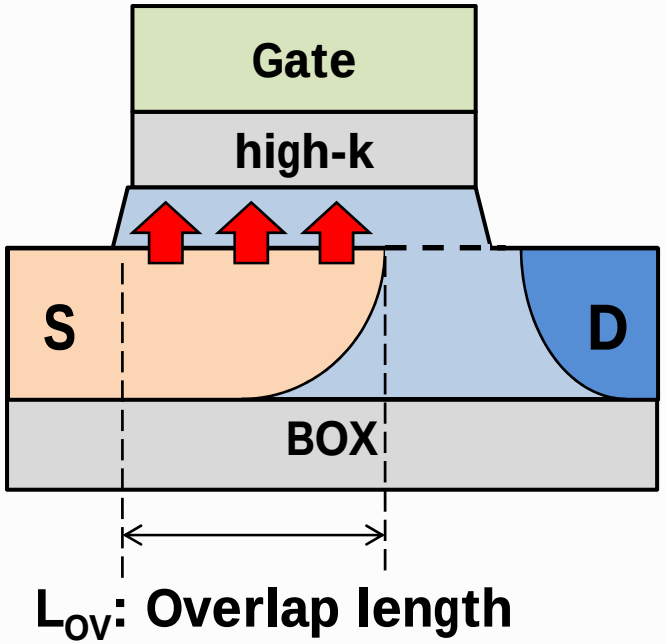
Lateral & vertical TFETs

- **Two TFET architectures**

Lateral (conventional) TFET



Vertical (parallel electric field) TFET



L_{OV}: Overlap length

BTBT is limited in interface
-->> Small I_D

BTBT area is enlarged

C. Hu et.al., VLSI-TSA 2008, 14 (2008)
R. Li et.al., Phys. Status Solidi C 9, 389 (2012)
Y. Morita et.al, Jpn. J. Appl. Phys. 52, 04CC25 (2013)

Objective of this work

- **Performance of the parallel electric field TFET (PE-TFET), relation between ON current and overlap length, is analyzed.**

- **Proposal of modified TFET architecture to improve electrostatics (Synthetic electric field TFET)**

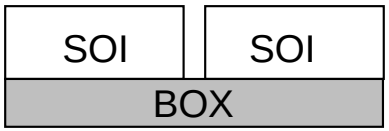
Performance of the PE-TFET

Fabrication of PE-TFET with epichannel

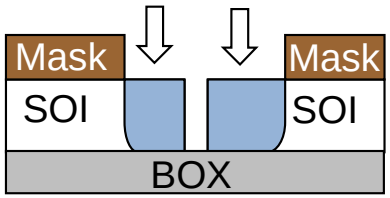
S/D first & "Junction-last" TFET process

- SOI mesa etching (a)
- P I/I (b)
- BF_2 I/I (c)
- Activation (1000 ˚C)
- Si epitaxial growth, high-*k* and gate (d)
- Gate stack etch (e)
- Contact
- Sintering

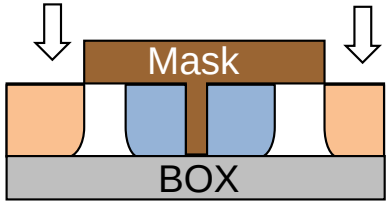
(a) SOI mesa etching



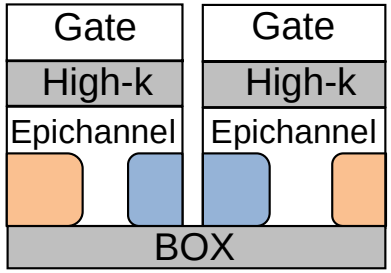
(b) P ion implantation



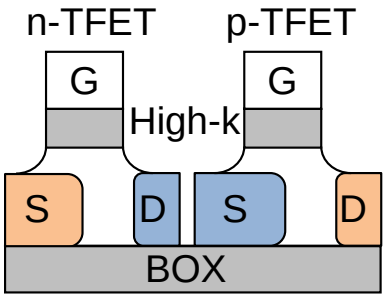
(c) BF_2 ion implantation

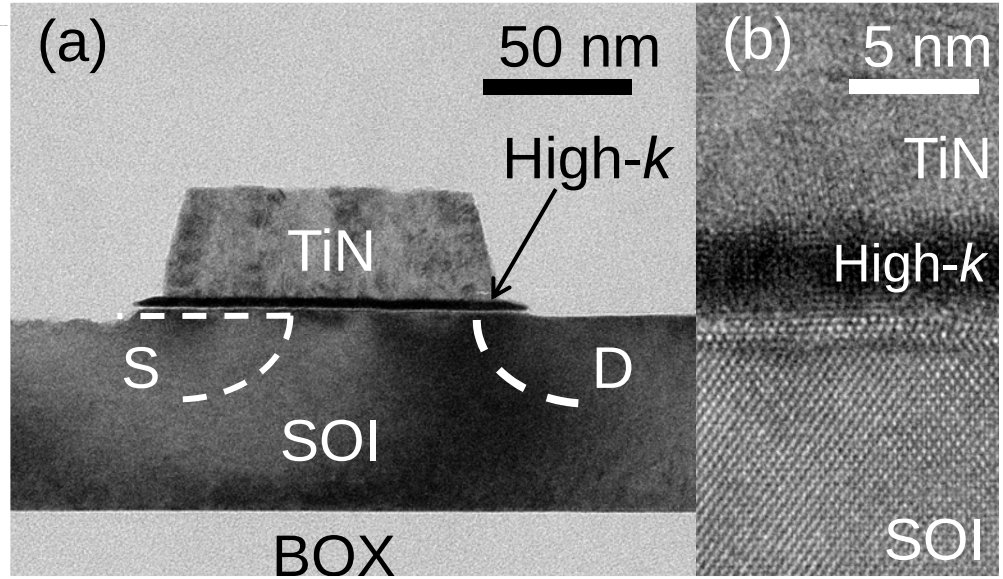


(d)

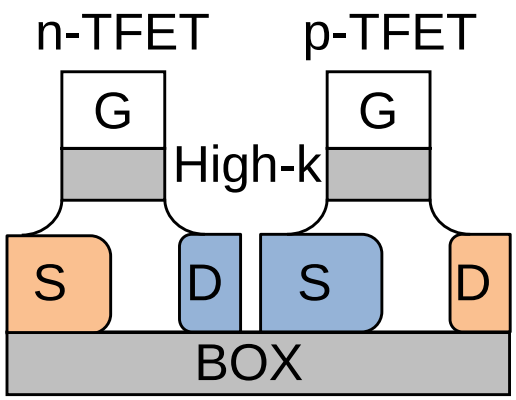


(e)

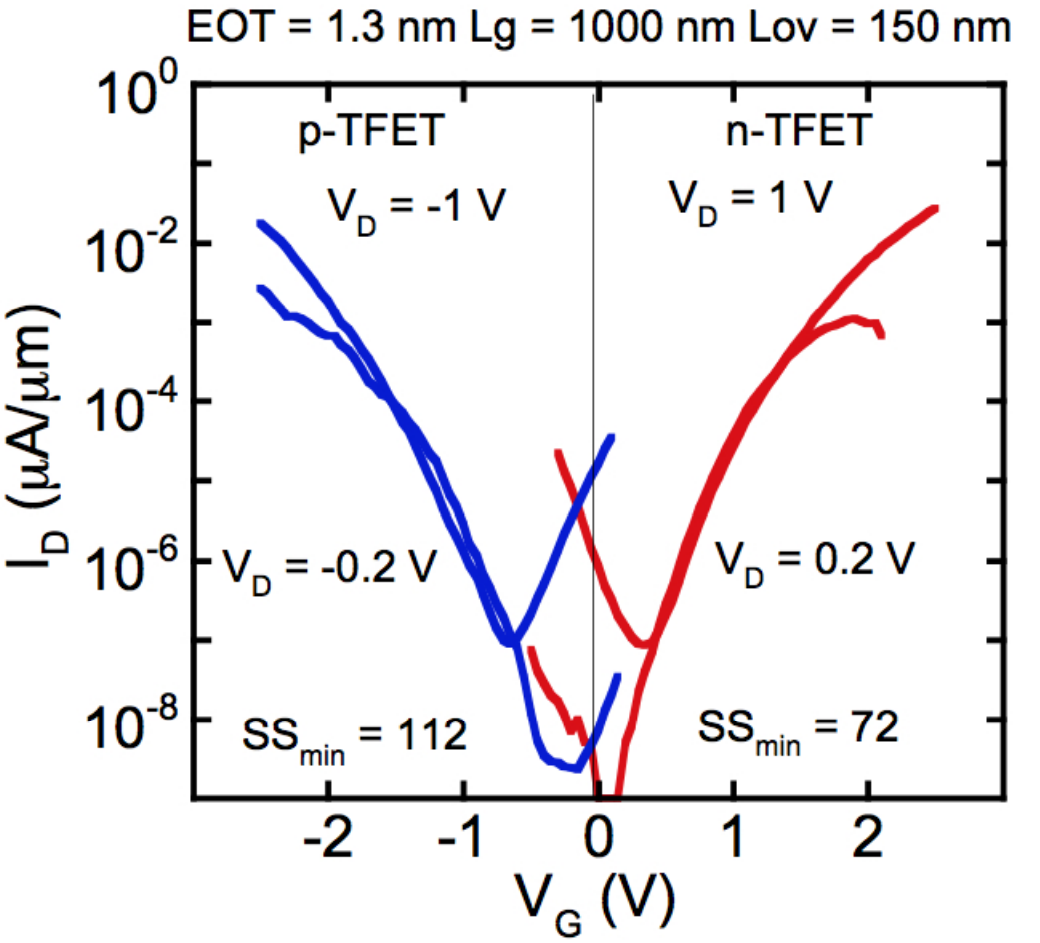




Operation of p- & n-PE-TFETs

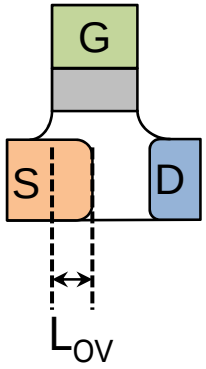


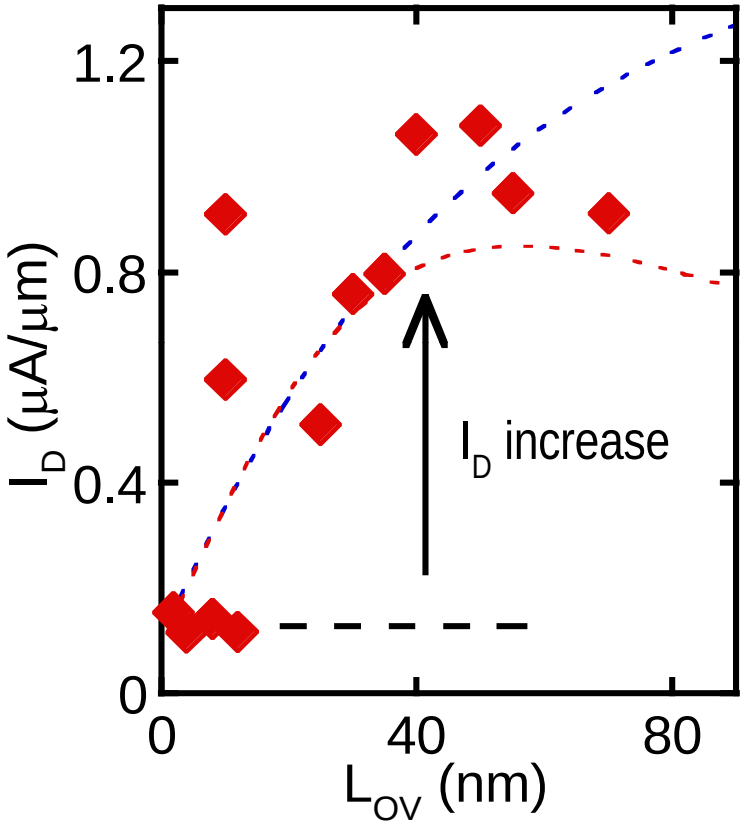
I_D-V_G

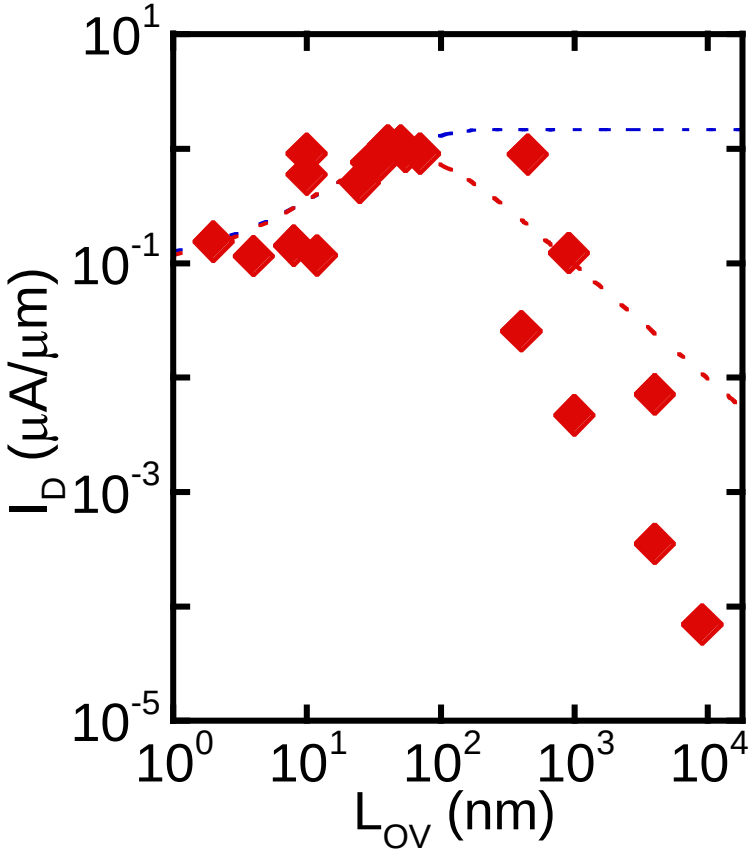


Effect of L_{OV} increase

Relation between I_D and L_{OV}



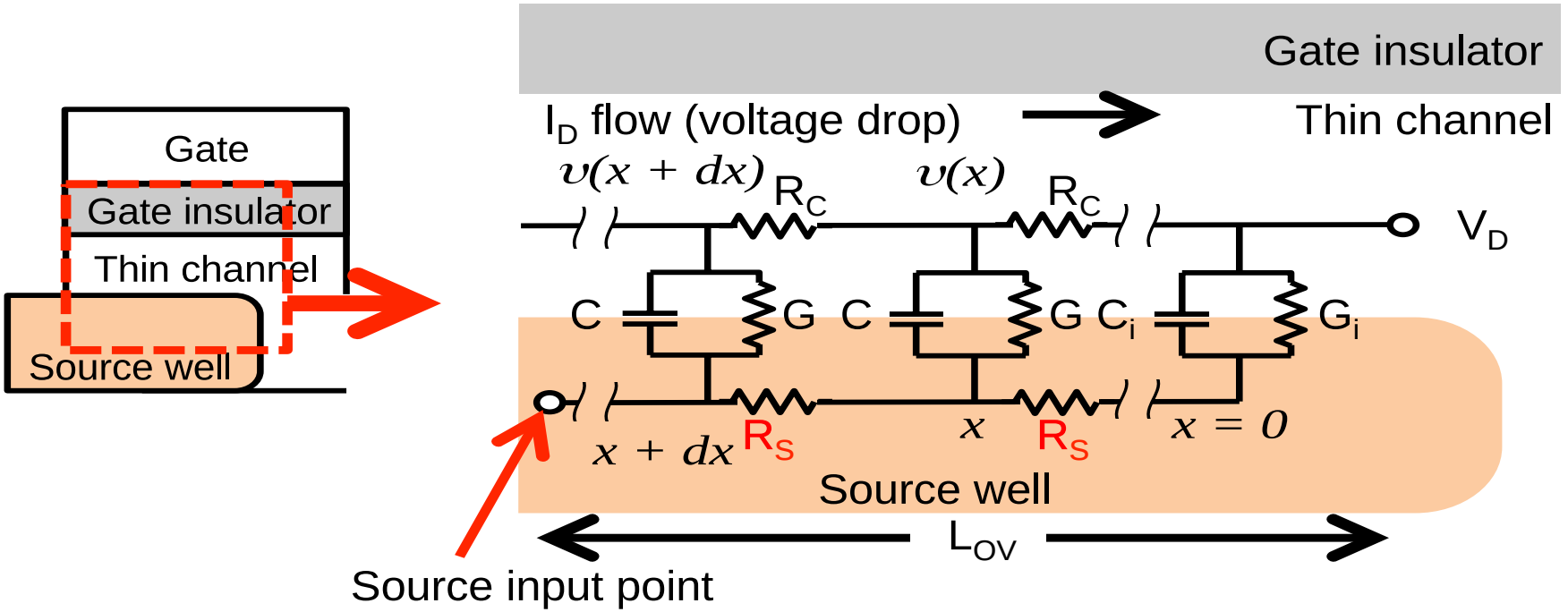




Confirming I_D increase with increasing L_{OV}
ON current degraded at L_{OV} > 1000 nm

Effect of L_{OV} increase

Analysis using a distributed-element circuit

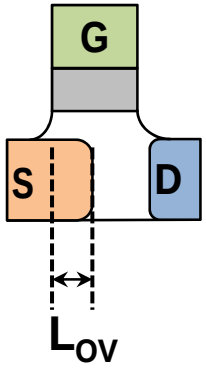


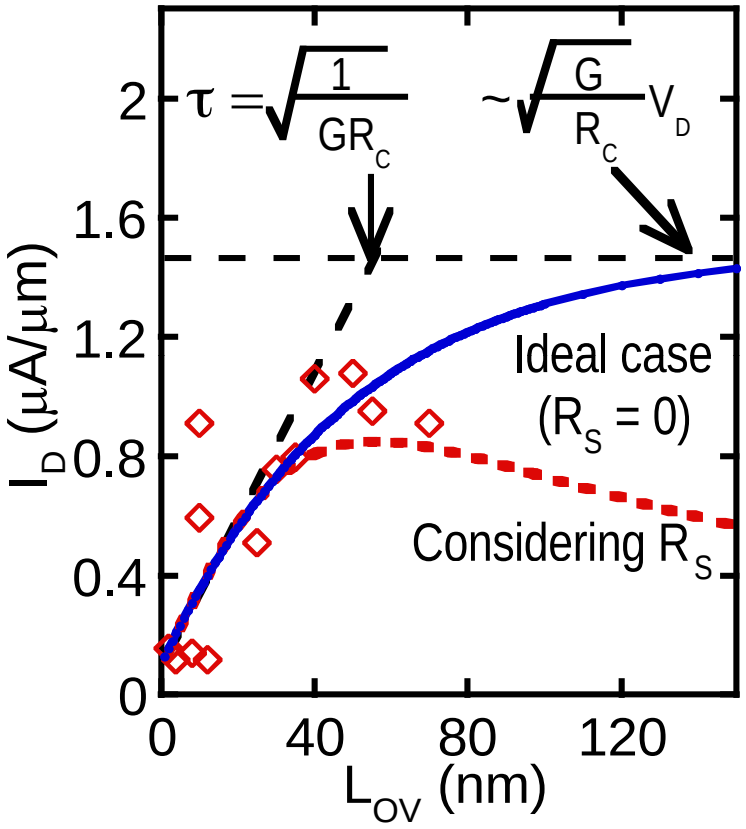
In ideal case (R_S ~ 0),
***i-v* relation can be describes as,**

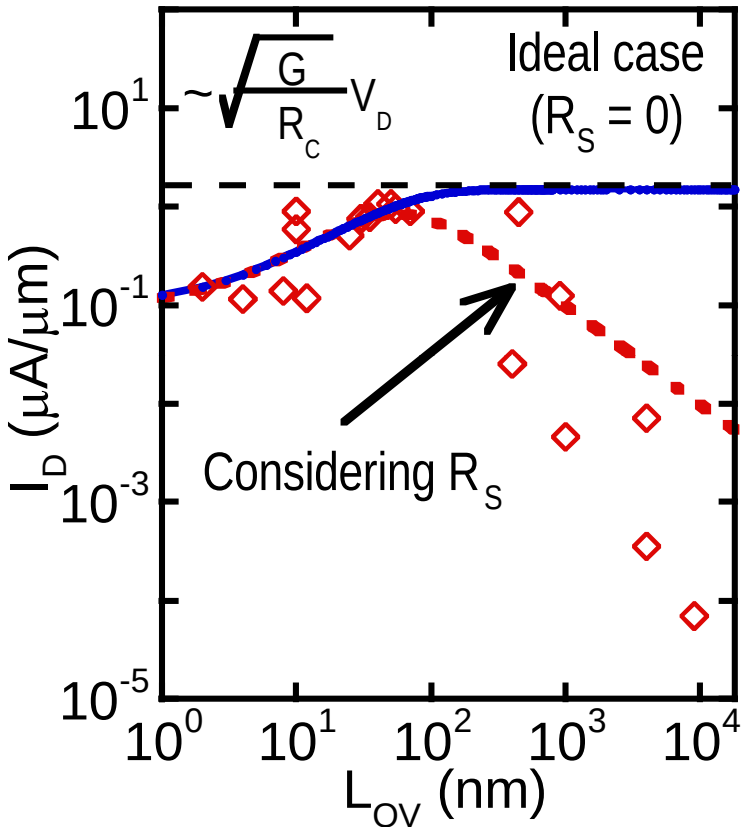
$$\begin{cases} -\dfrac{dv(x)}{dx} = R_c i(x) \\ -\dfrac{di(x)}{dx} = G v(x) \end{cases}$$

Effect of L_{OV} increase

Relation between I_D and L_{OV}







Upper limit of ON current ! $\sim \sqrt{\frac{G}{R_C}} V_D$

Experimental results

Limit of drain current in PE-TFET

$$I_{ONMAX} \sim \sqrt{\frac{G}{R_C}} V_D$$

-->> Self-voltage-drop effect in thin channel

Trade off

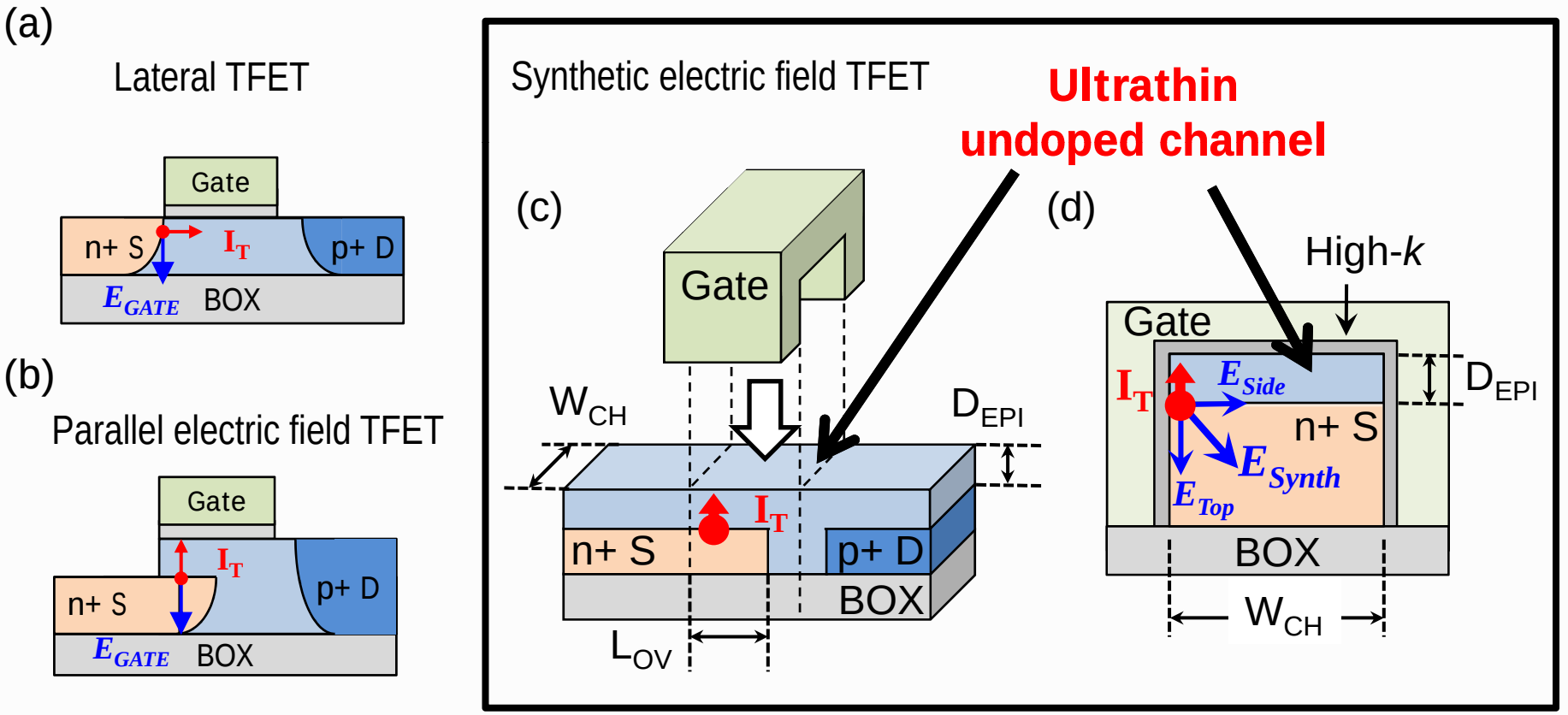
Enhancing G <<-->> Reducing R_C

Balance between tunnel conductance and channel resistance is critical.

Proposal of modified TFET architecture

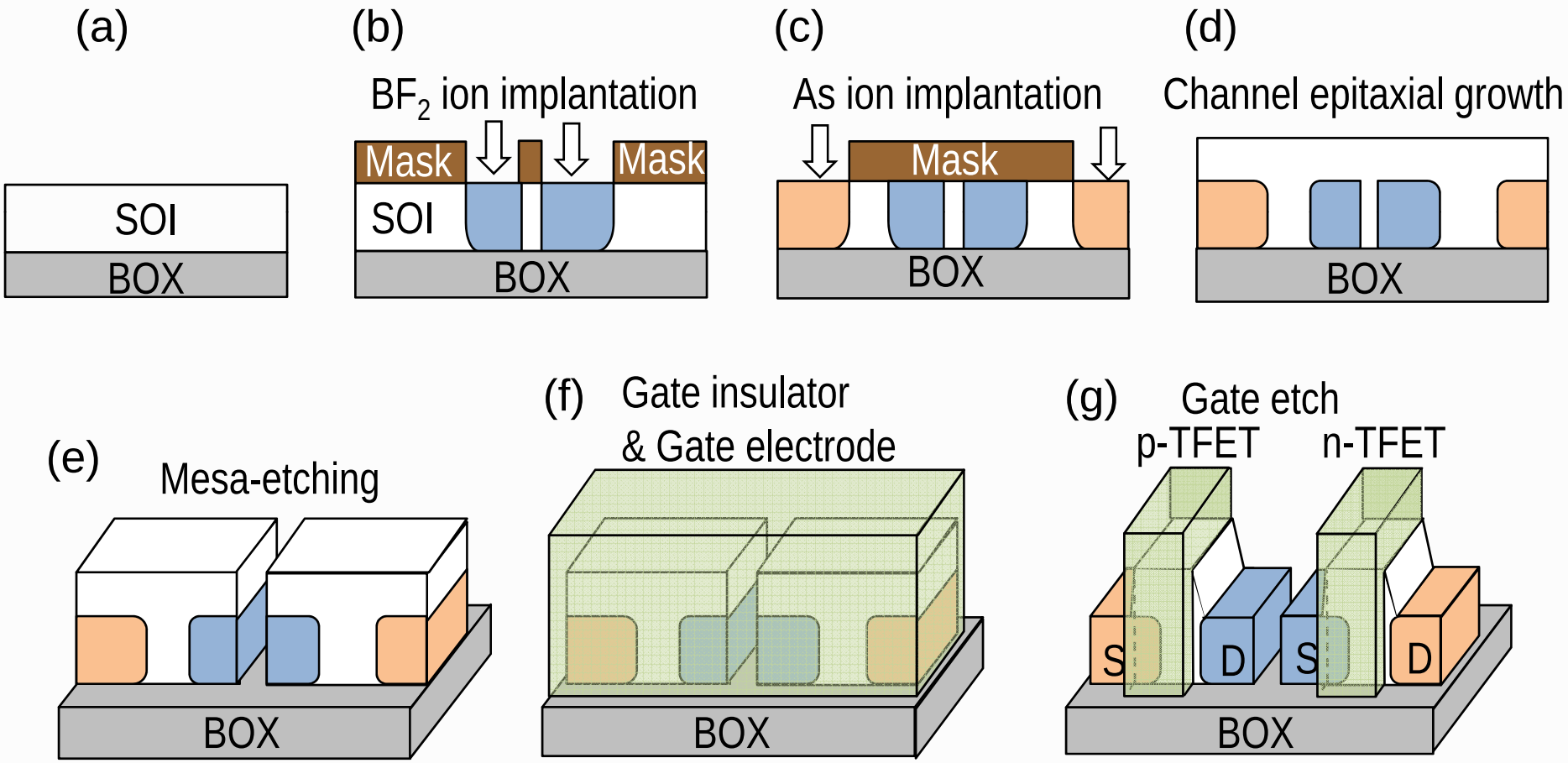
Proposal of synthetic electric field TFET

- **Multiplication of lateral & vertical electric fields**



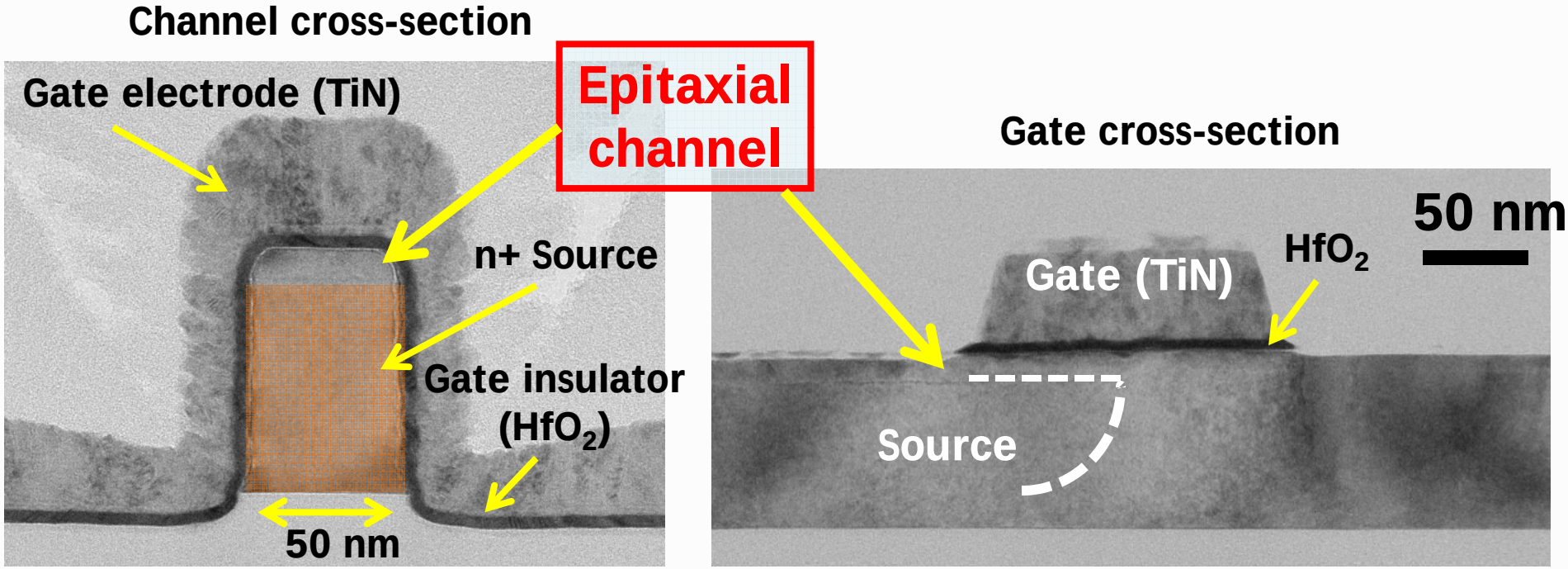
Fabrication of SE-TFET with epichannel

- **Based on source/drain-first CMOS process**

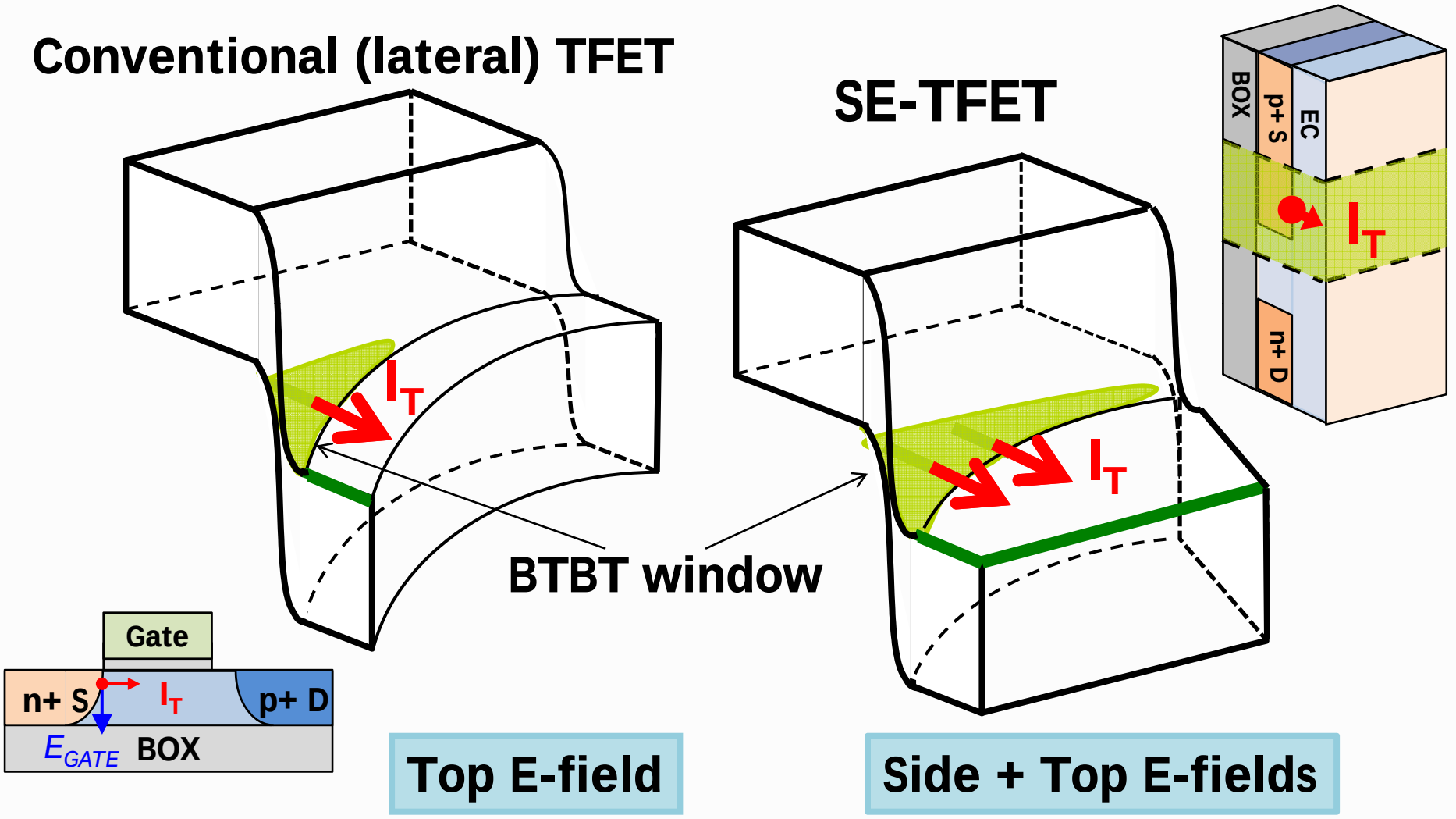


Device structures

- **Small amount of defects at epitaxial channel/source interface**



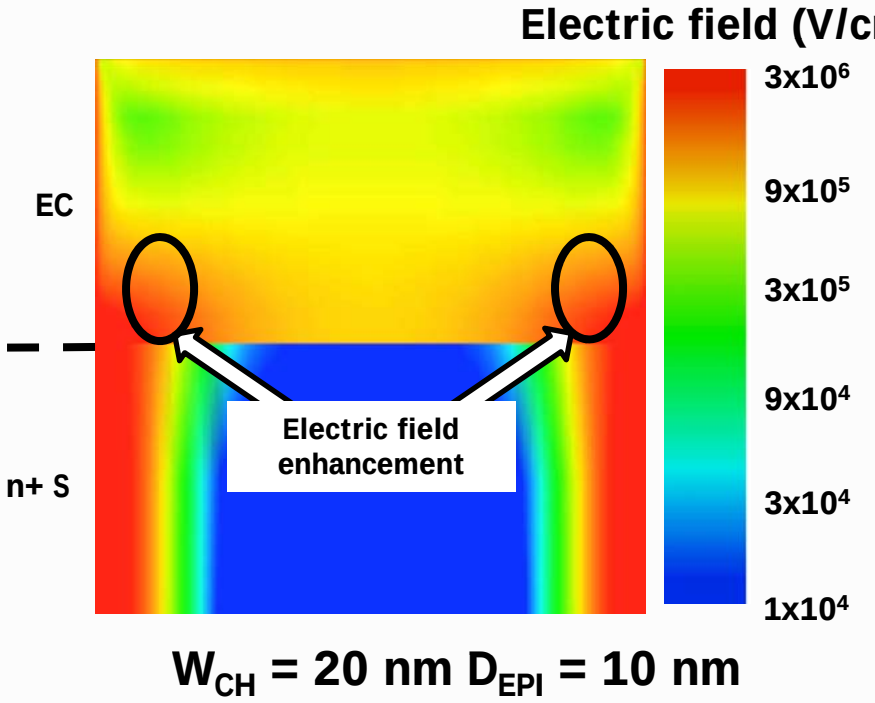
Operation mechanism



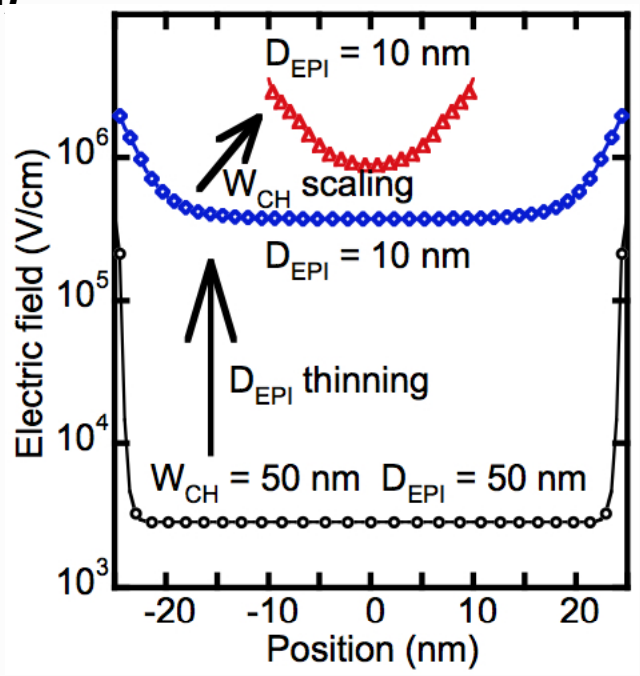
Simulation of electric field

- **Electric field at edges is enlarged by SE-effect.**
- **Scaling of channel thickness and width enhances SE-effect**

Electric field distribution

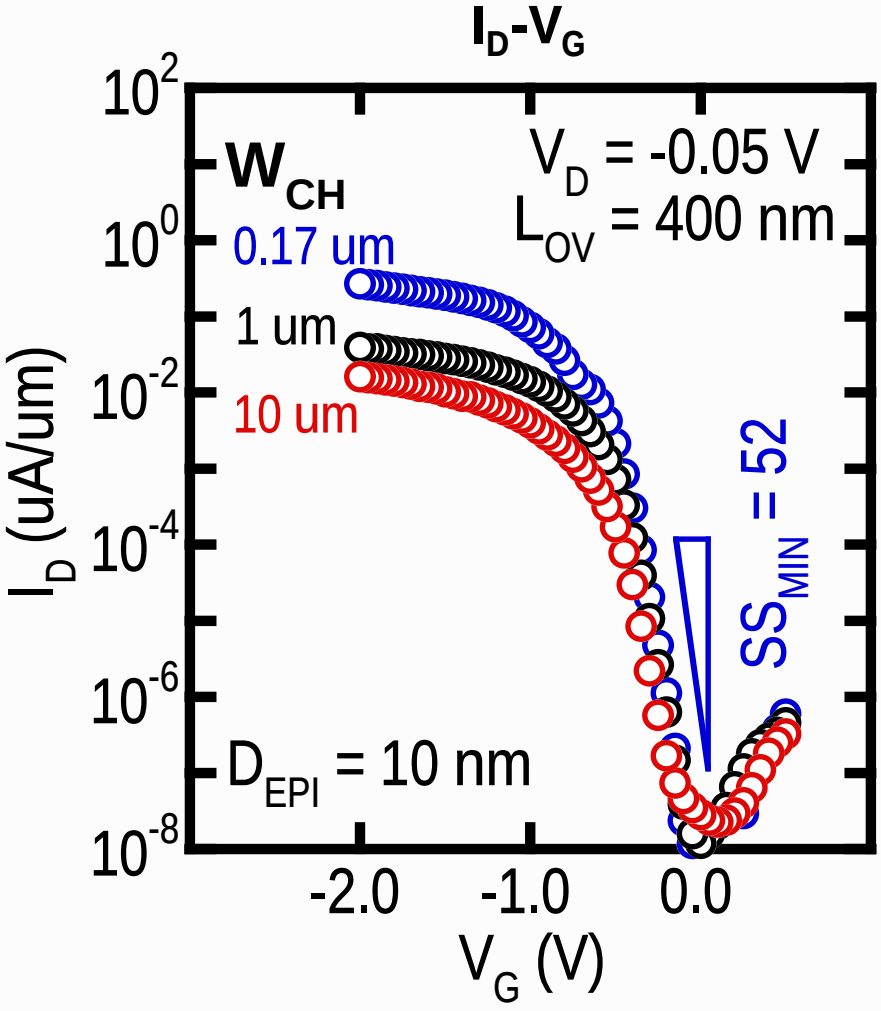


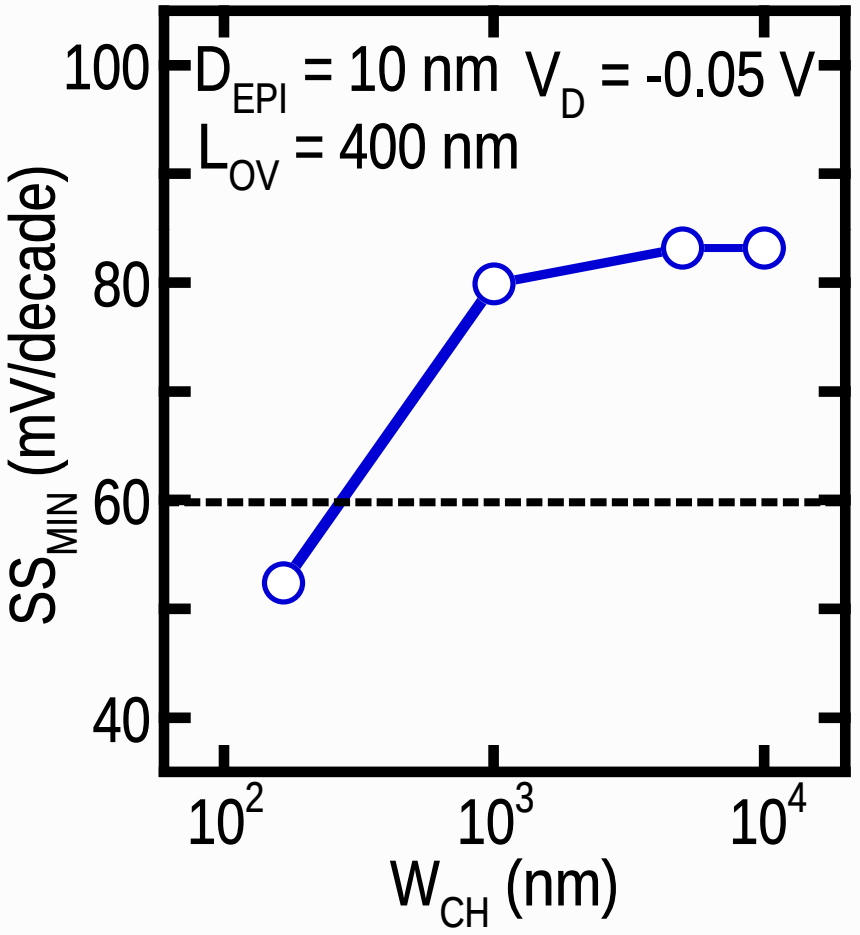
W_{CH} = 20 nm D_{EPI} = 10 nm



Impact of channel width

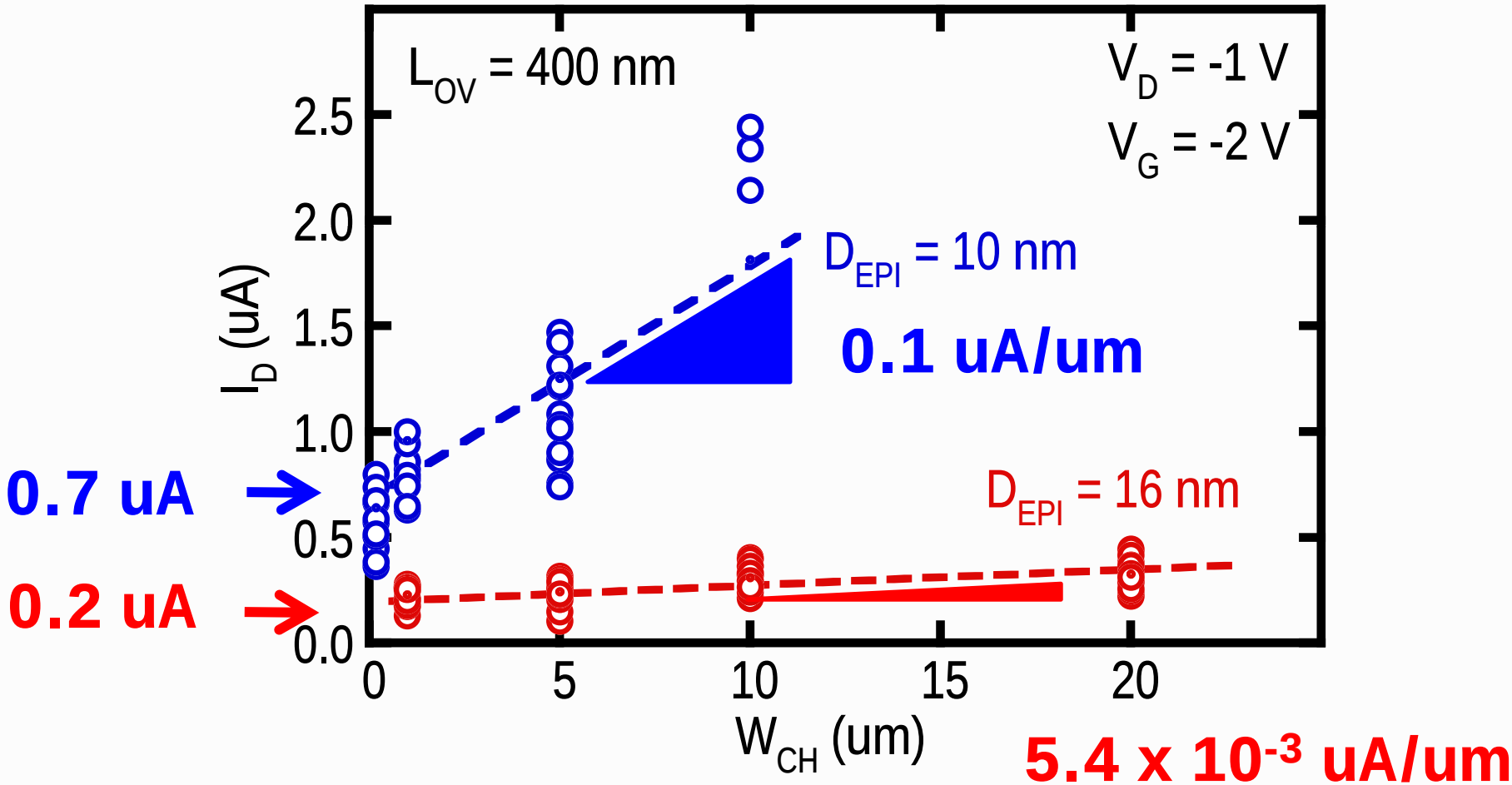
- **Better performance in narrower channel device**





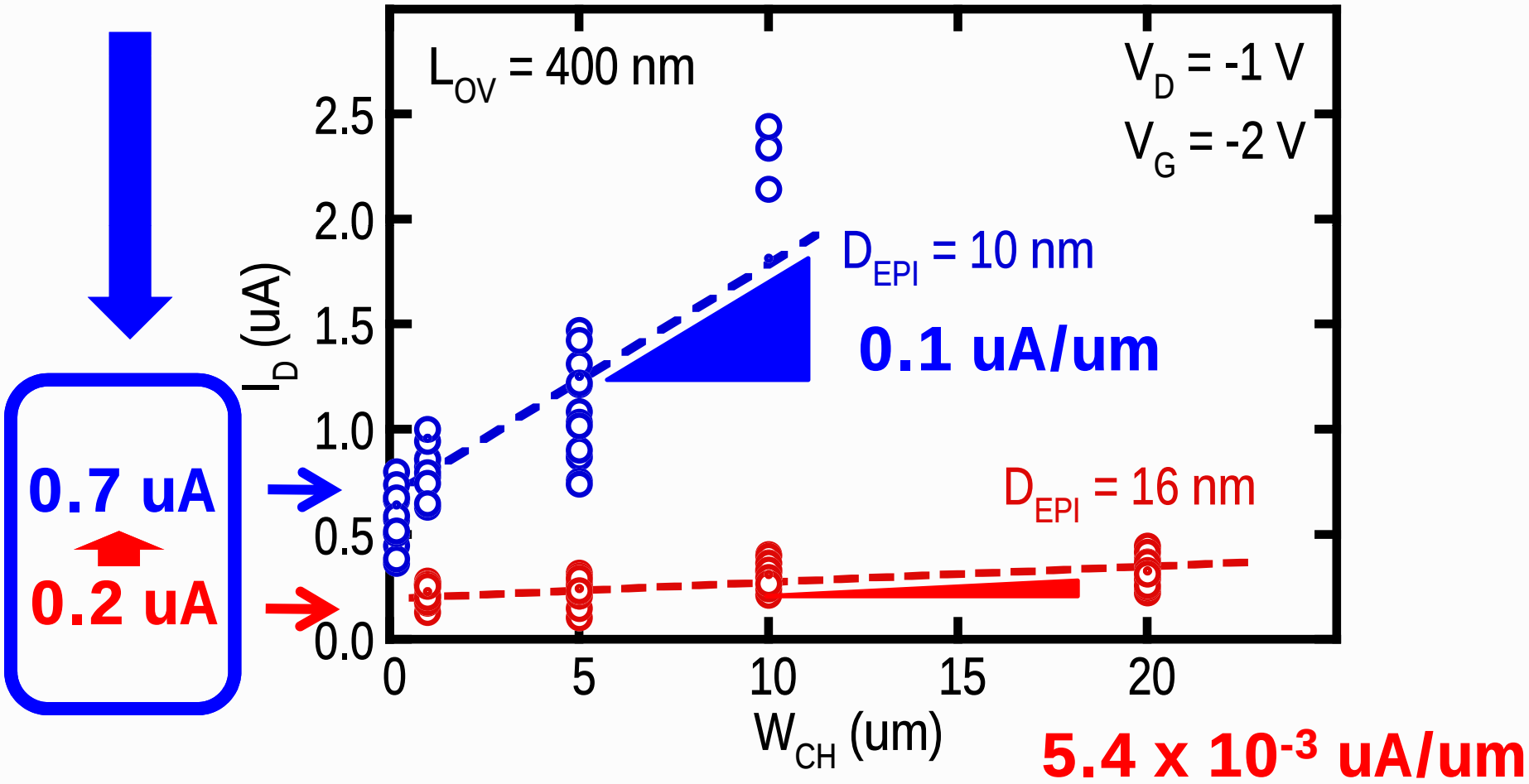
Impact of channel width

- I_D at W_{CH} = 0 corresponds to the **edge current**.



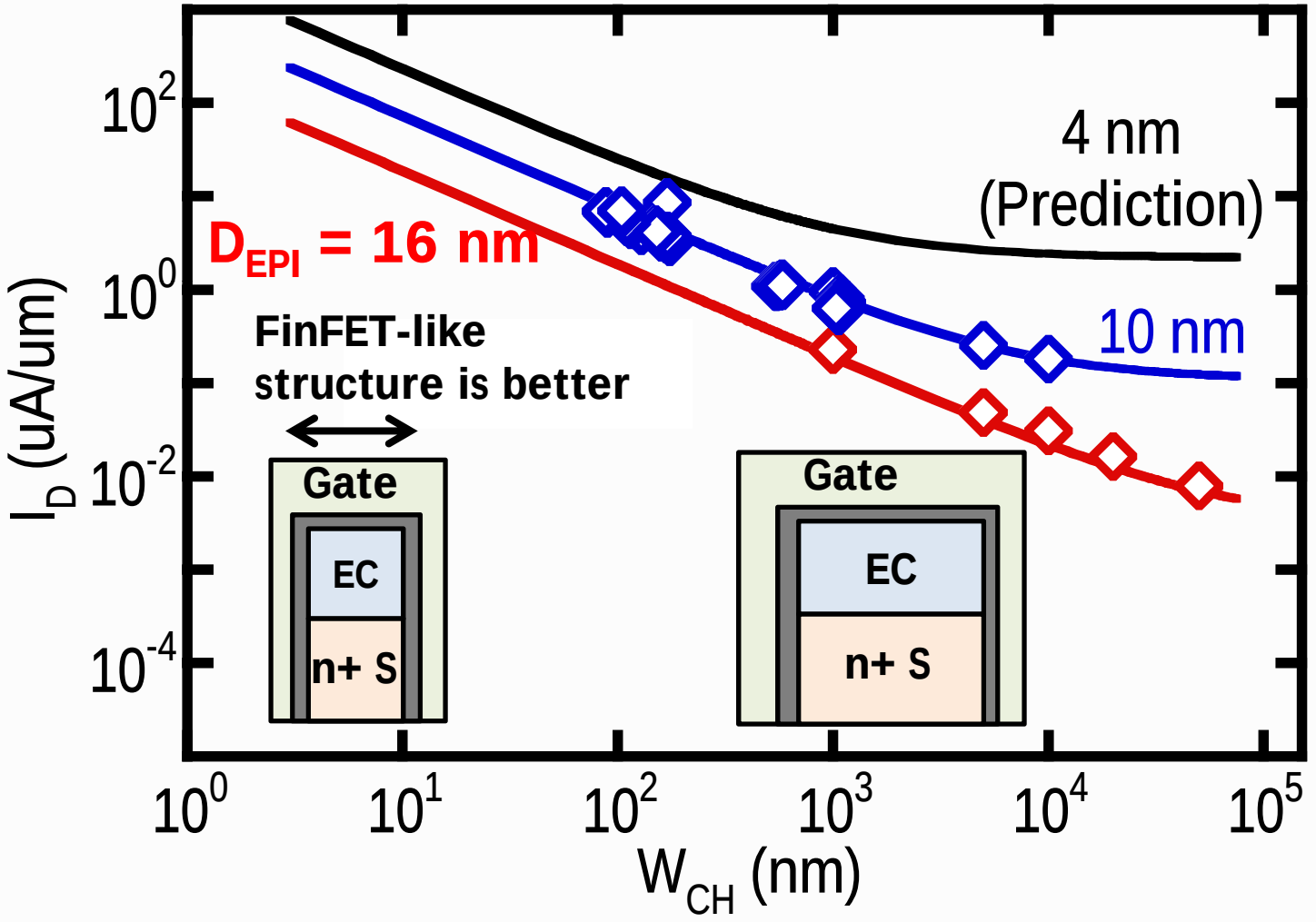
Impact of channel width

- **Edge current is enhanced by D_{EPI} scaling.**

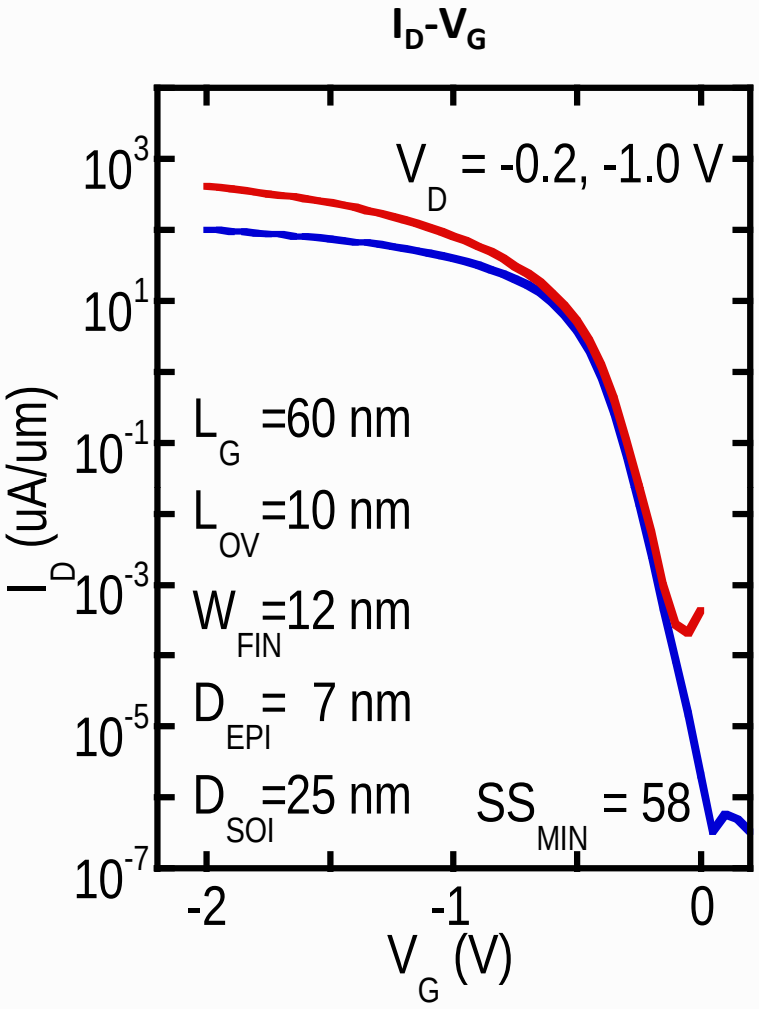


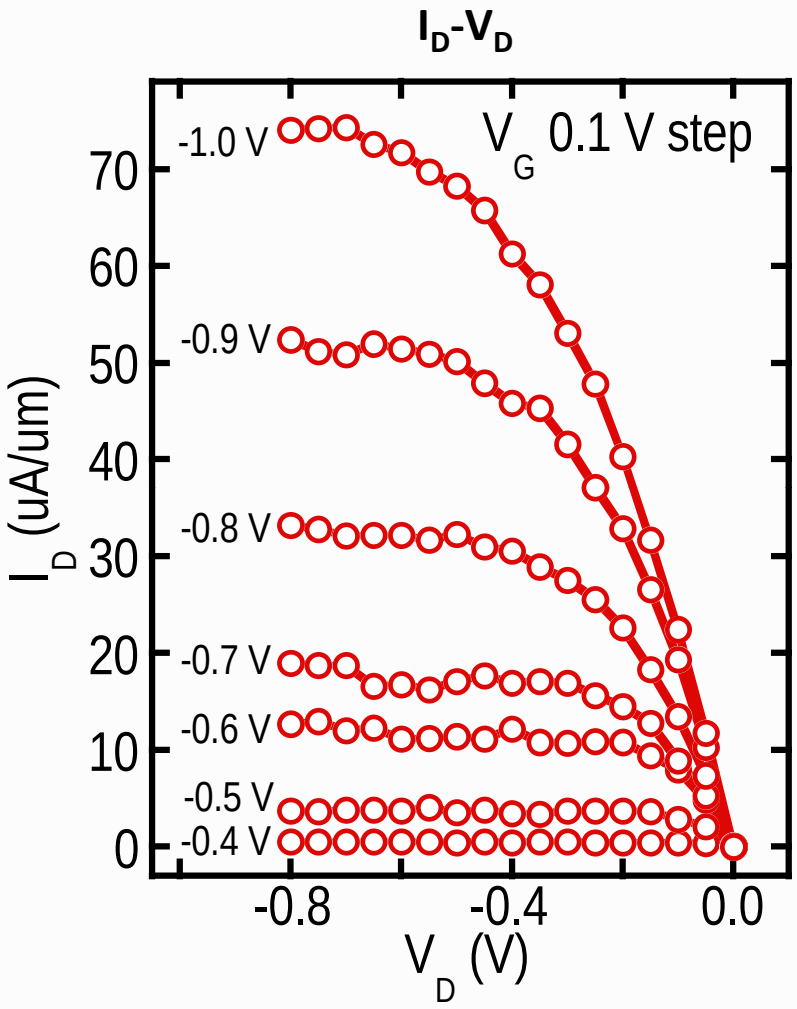
Impact of channel width

- **Scaling of both D_{EPI} and W_{CH} enhance performance**



Performance of SE-tunnel FinFET





Significant performance

SS_{MIN} = 58, I_D = 4 uA/um @(V_G,V_D)=(-0.5,-0.2 V)

400 uA/um @(V_G,V_D)=(-2,-1 V)

Summary

Parallel electric field TFET

- Limit of ON current
- Balance between tunnel conductance and channel resistance is critical

Synthetic electric field TFET

- Scaling induced performance enhancement
- FinFET-like slim device is promising.
- Significant performance in small voltage

  SS_{MIN} = 58, I_D = 4 uA/um @(V_G,V_D)=(-0.5,-0.2 V)

  400 uA/um @(V_G,V_D)=(-2,-1 V)

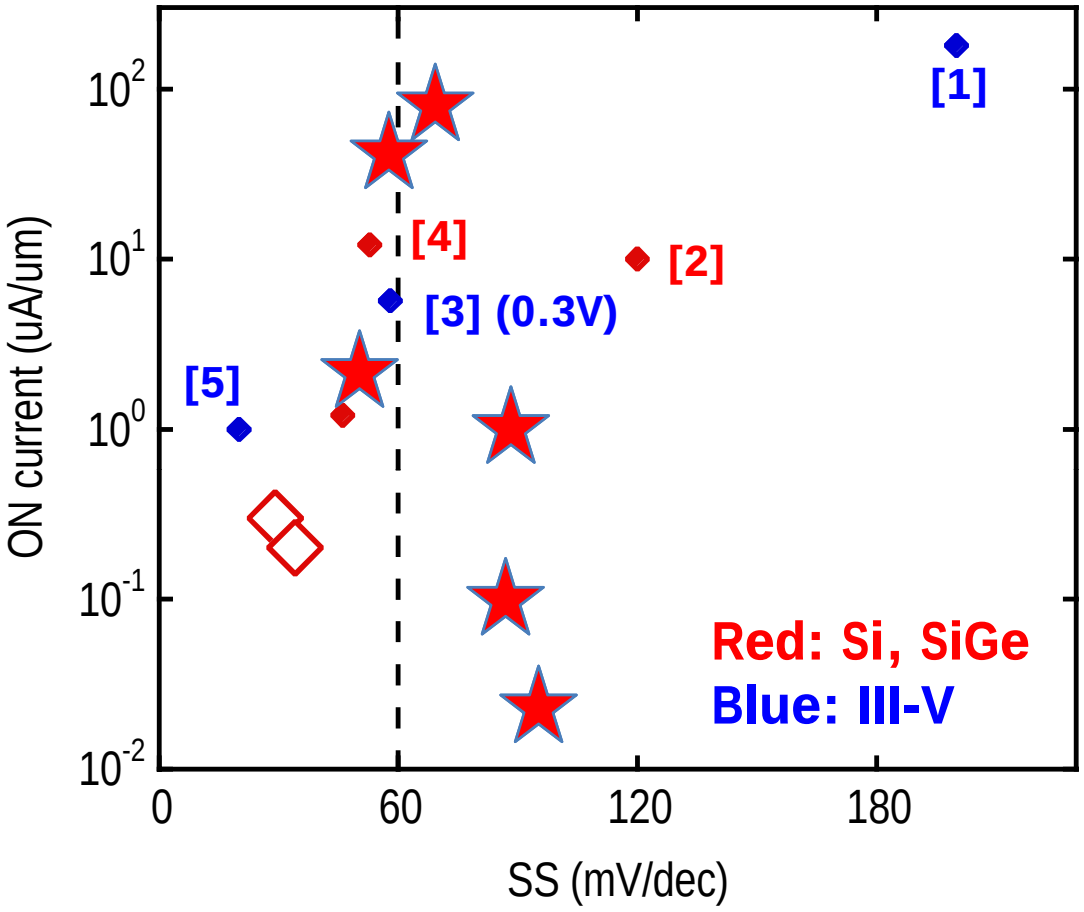
- The concept can be applicable to Ge or III-V TFETs.

Acknowledgement

This research was supported by JSPS through the First Program, "Development of Core Technologies for Green Nanoelectronics".

Thank you for your kind attention.

Benchmark

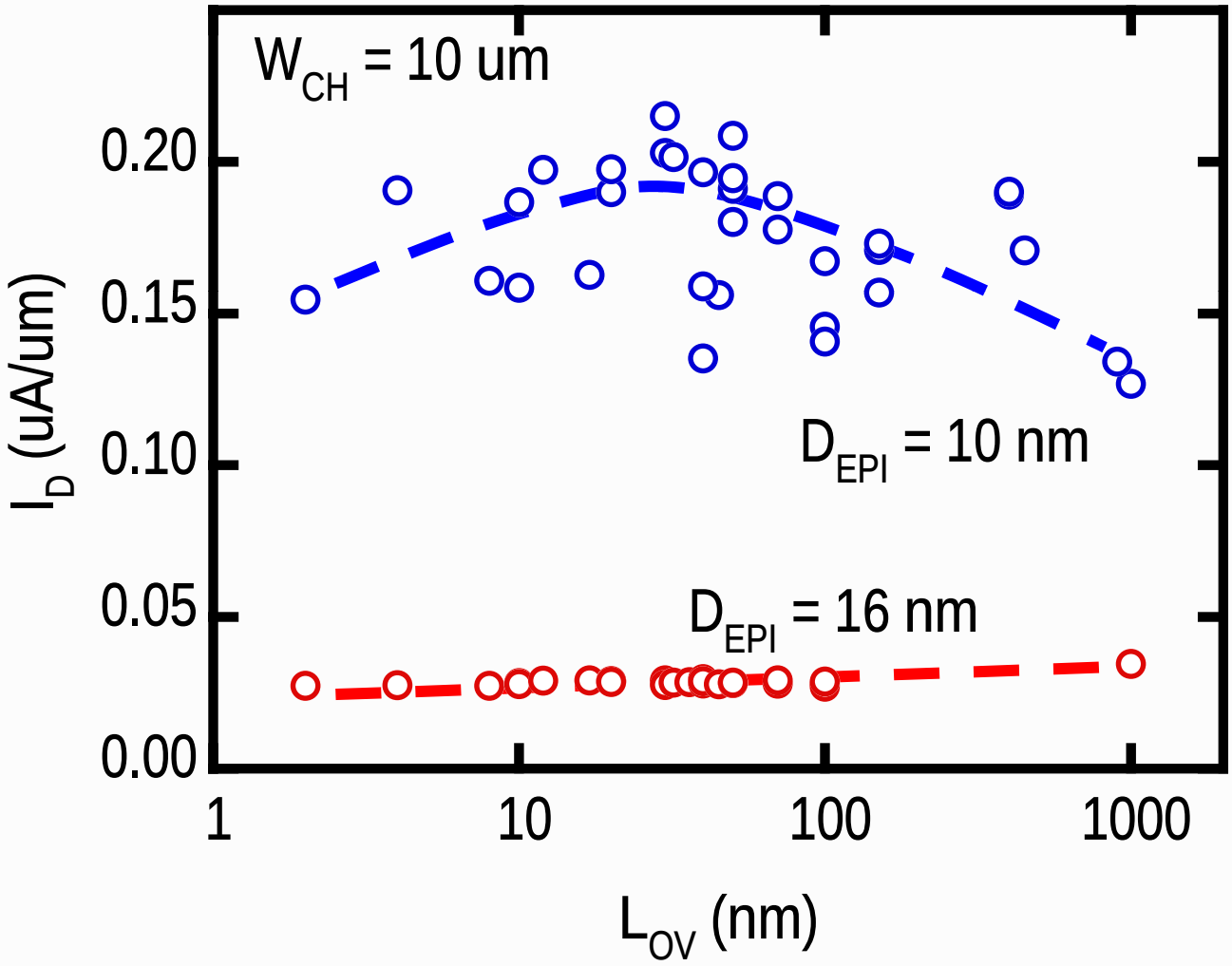


[1] *G. Zhou, et al., IEDM 2012*
[2] *A. Villalon, et al., VLSI2012*
[3] *G. Dewey, et al., IEDM 2011*
[4] *W. Choi,et al., EDL28 2007*
[5] *K. Tomioka, et al., VLSI2012*

Our data
(No strain, no Ge, no metal SD, only by device consideration)

Impact of L_{OV}

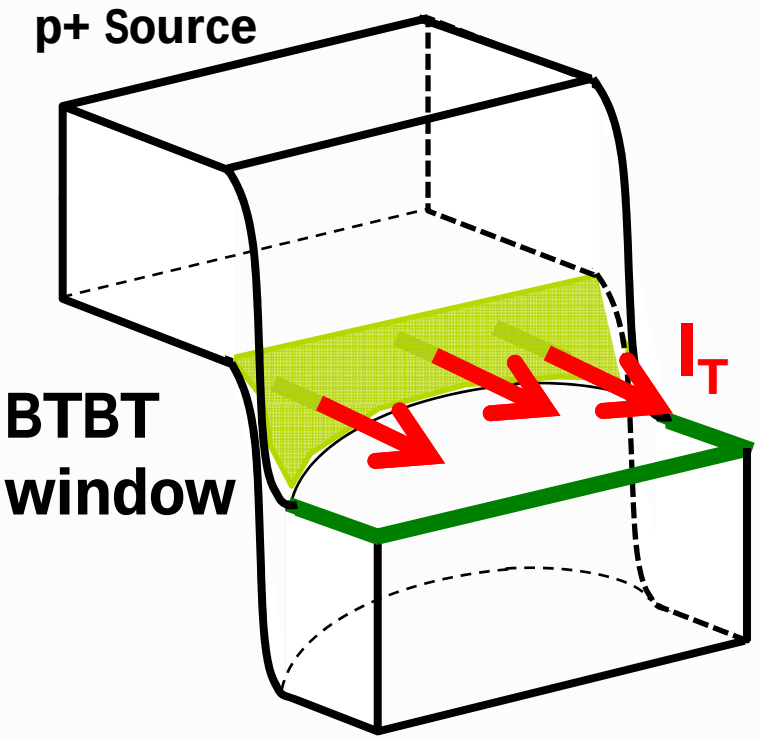
- **Maximum I_D at L_{OV} ~ 50 nm**

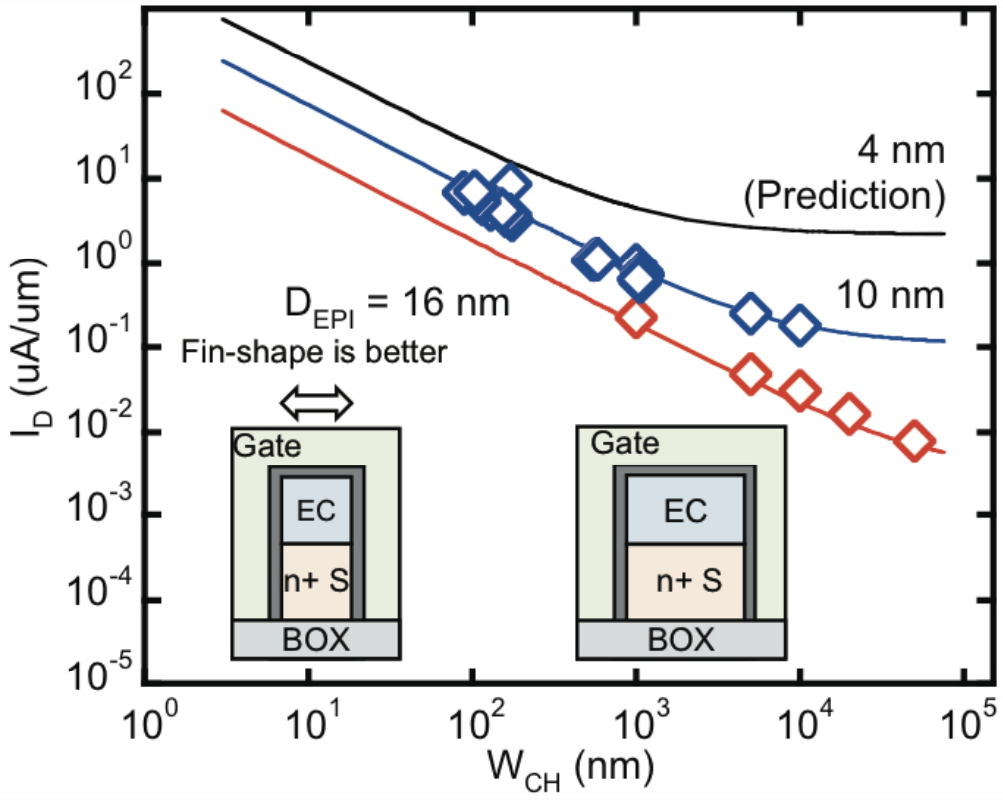


Scaling of channel width

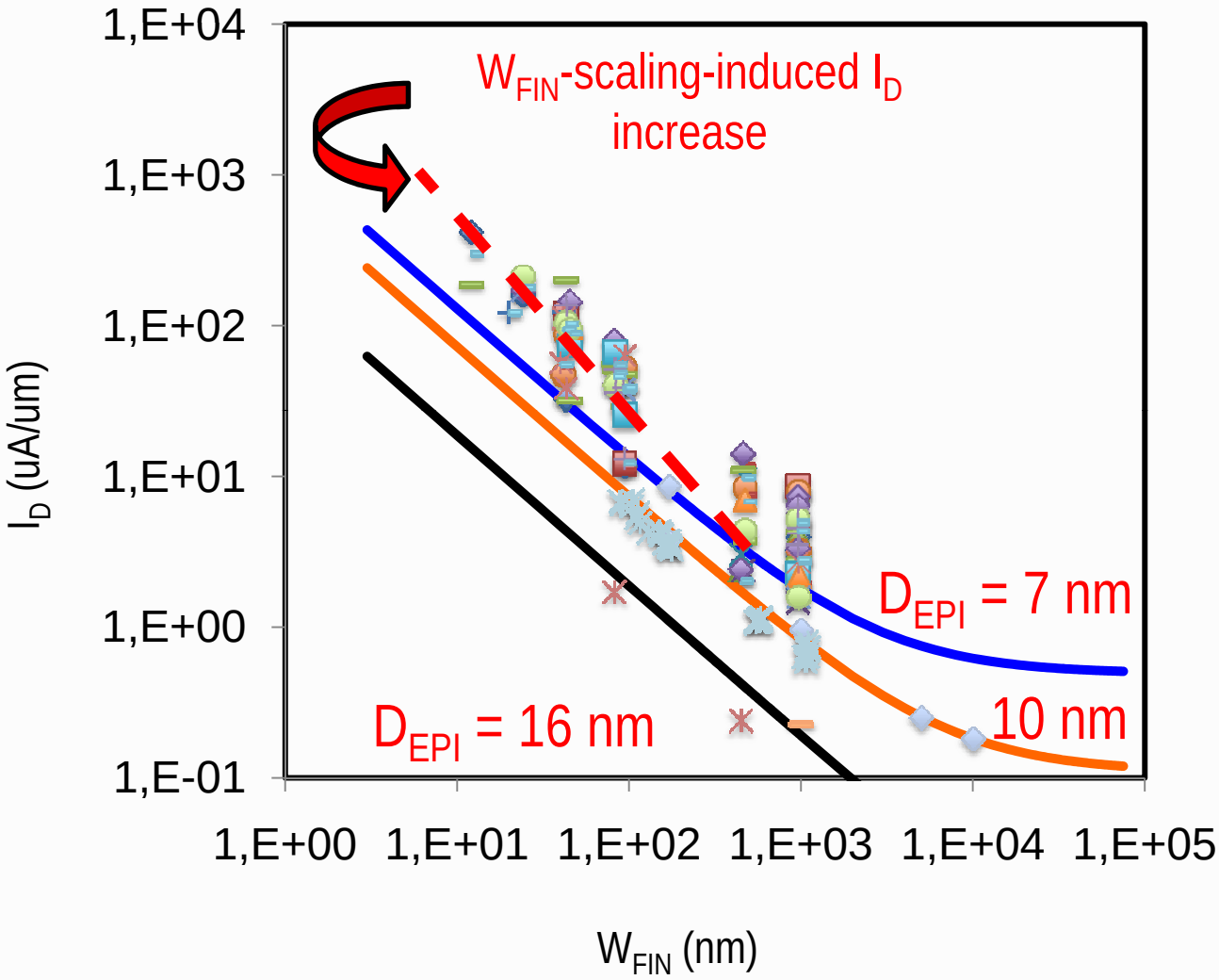
- Scaling of both D_{EPI} and W_{FIN} enhance performance.

SE-tunnel FinTFET



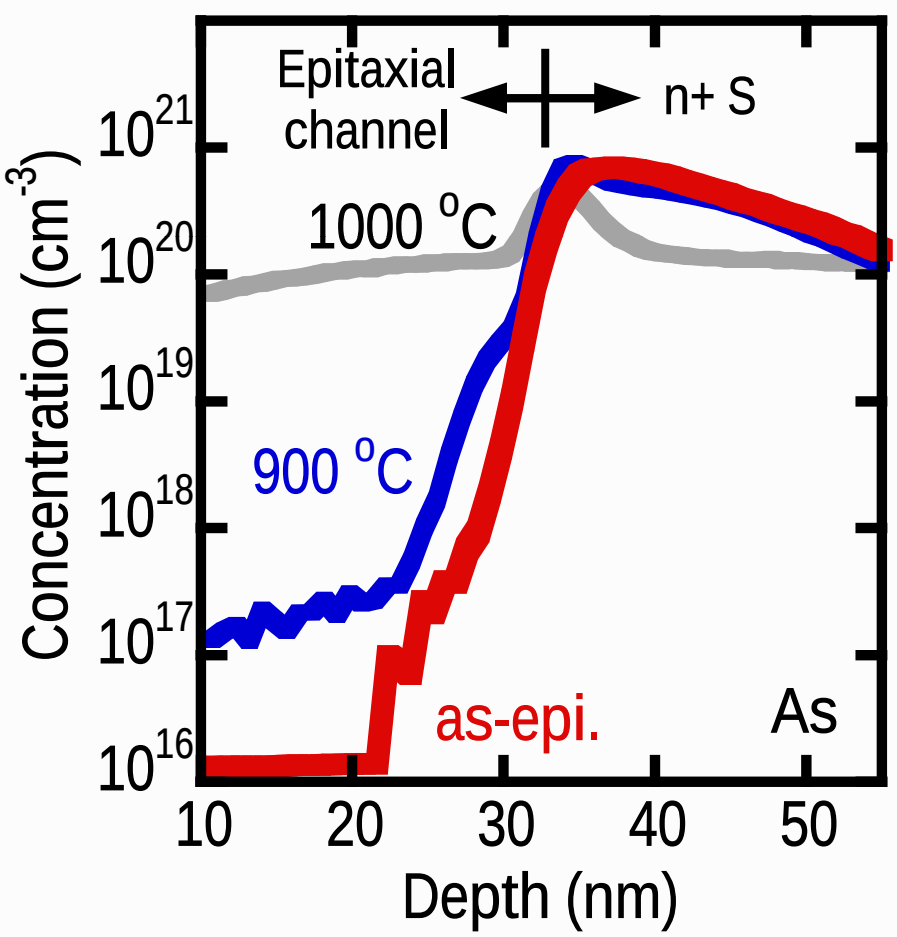


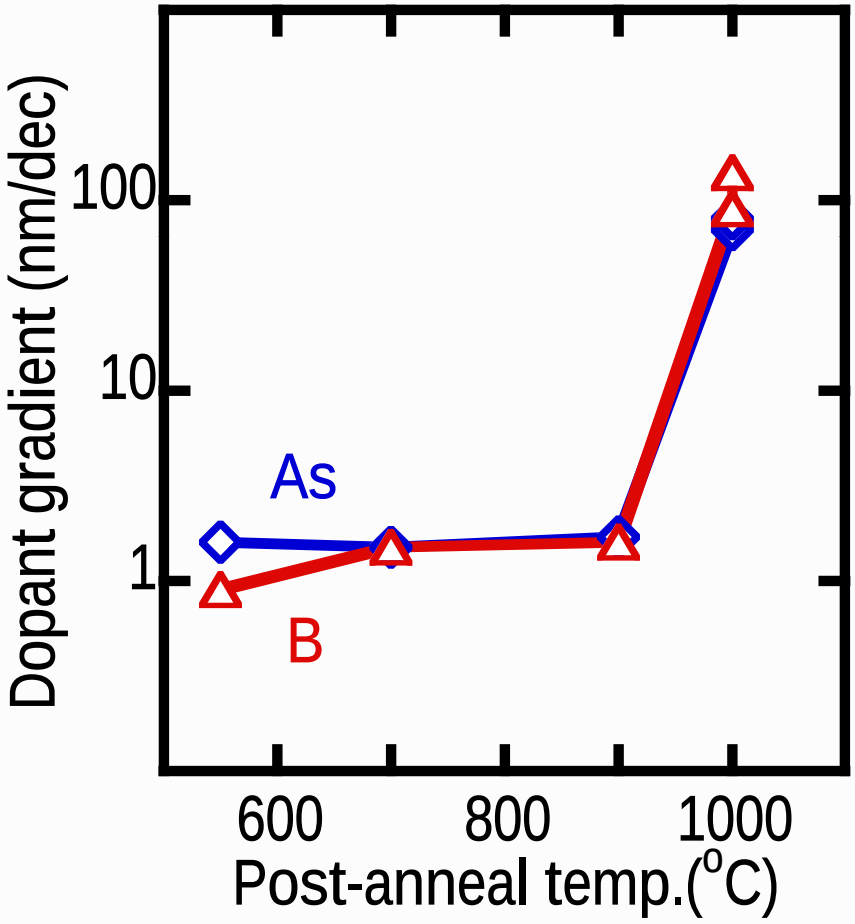
Both Sides + Top E-fields


1,E+04
1,E+03
1,E+02
1,E+01
1,E+00
1,E-01
I_D (uA/um)
W_{FIN}-scaling-induced I_D increase
D_{EPI} = 7 nm
10 nm
D_{EPI} = 16 nm
1,E+00 1,E+01 1,E+02 1,E+03 1,E+04 1,E+05
W_{FIN} (nm)

SIMS analysis of dopant profiles

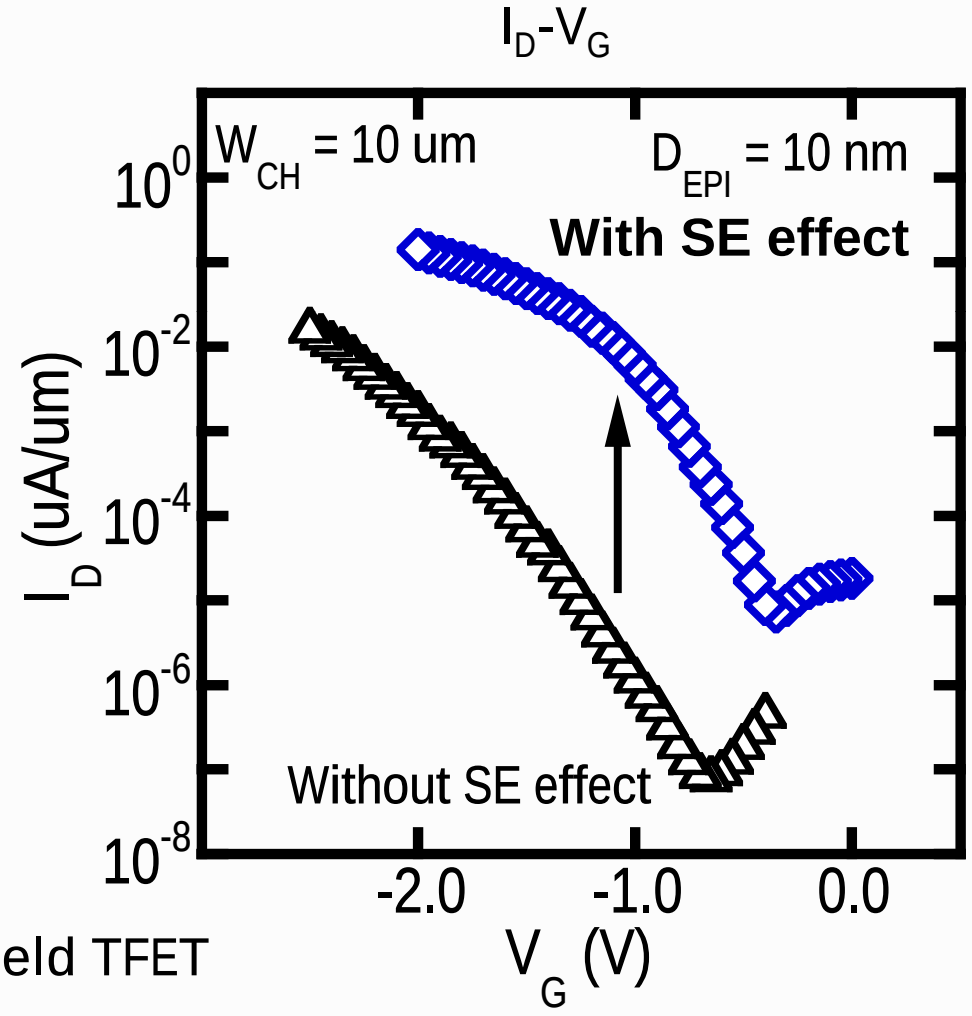
- Dopant steepness in the epitaxial channel is maintained below 900 ˚C.

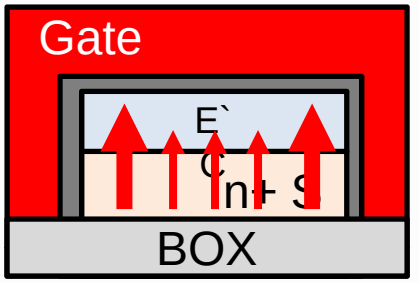




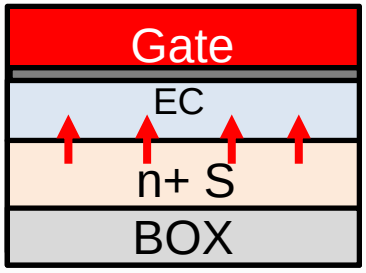
Impact of SE effect

- Significant increase of I_D in the SE-TFET





SE-TFET

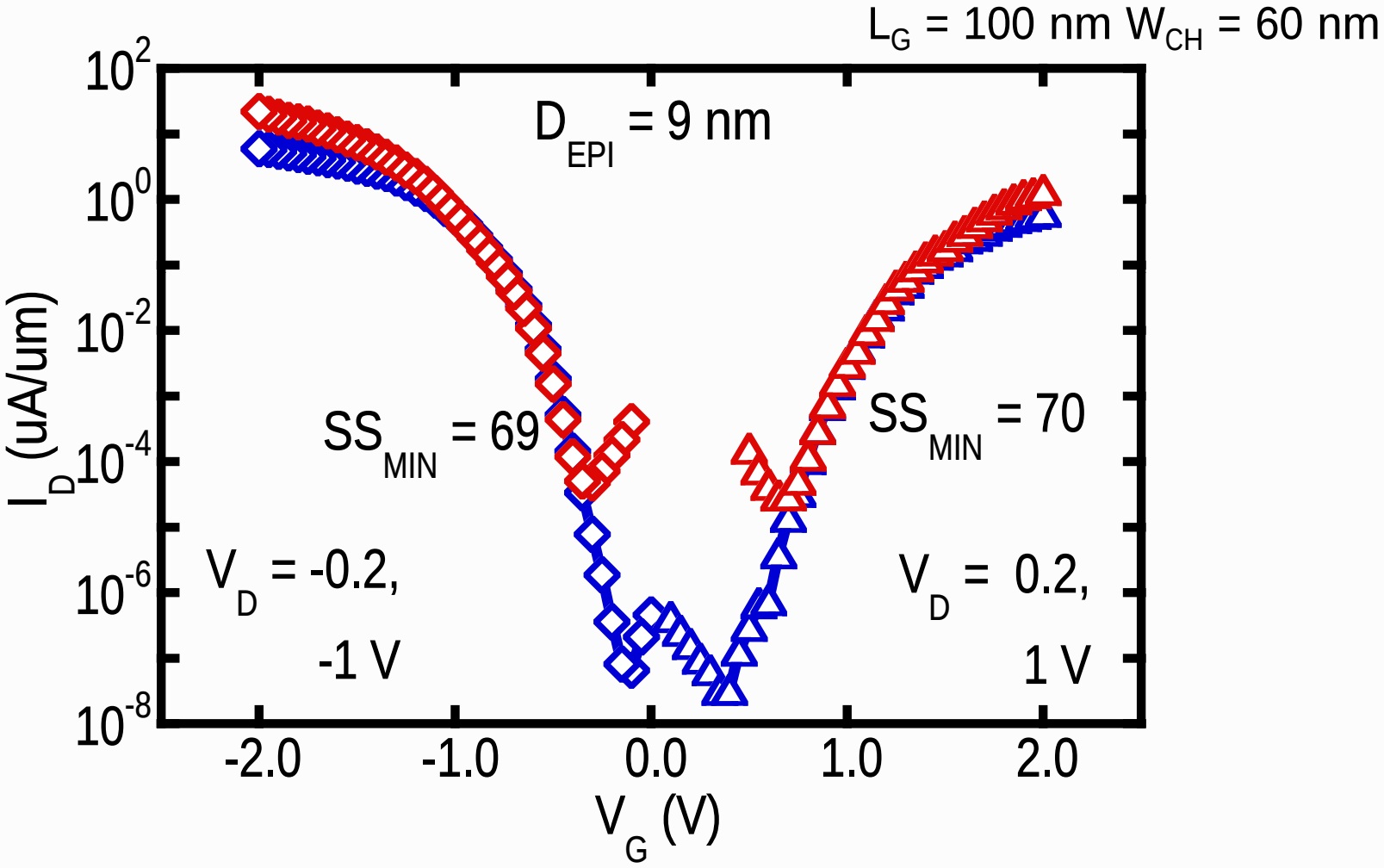


Parallel electric field TFET

	This work	This work	This work	This work	Villalon et al VLSI2012 [8]	Villalon et al VLSI2012 [8]	Knoll et al EDL2013 [9]	Zhou et al IEDM2012 [10]	Zhou et al IEDM2012 [10]	Dewey et al IEDM2011 [11]
Types	p	p	p	p	p	p	p	n	n	n
Materials	Si	Si	Si	Si	SiGe30%	SiGe30%	Si	GaSb/InAs	GaSb/InAs	InGaAs
Structures	DL Fin	DL Fin	DL Fin	DL Fin	ETSOI	ETSOI	Nanowire	Vertical	Vertical	Vertical
Boosters	DL Fin	DL Fin	DL Fin	DL Fin	Strain	Strain	Strain Metal S/D	III-V	III-V	III-V
V_D (V)	-1	-1	-0.2	-0.2	-1	-1	-0.5	1	0.5	0.3
V_G (V)	-2	-1	-1	-0.5	-2	-1	-1	1	0.5	~0.48
V_{ON}-V_{OFF} (V)	-2	-1	-1	-0.5	-2	-1	-1	2	1.5	0.5
I_{ON} (uA/um)	417	82	40	4	~300	~10	~5	380	180	5.7
I_{MIN} (uA/um)	2.00E-04	2.00E-04	2.00E-06	2.00E-06	3.70E-05	3.70E-05	~2e-6	5.07E-02	3.00E-02	1.00E-04
I_{ON}/I_{MIN}	2.09E+06	4.10E+05	2.00E+07	2.00E+06	8.11E+06	2.70E+05	2.50E+06	7.50E+03	6.00E+03	5.70E+04
SS_{MIN} (mV/dec)	70	70	58	58	~120	~120	90	200	200	58
EOT (nm)	1.3	1.3	1.3	1.3	1.25	1.25	3 nm HfO_2	1.3	1.3	1.1
L_G (nm)	60	60	60	60	200	200	200	-	-	100

I_D-V_G of SE-TFETs

- Symmetric operation of p & n SE-TFETs



Tunability of L_{ov}

p-TFET
Lg = 1 um
Lw = 10 um

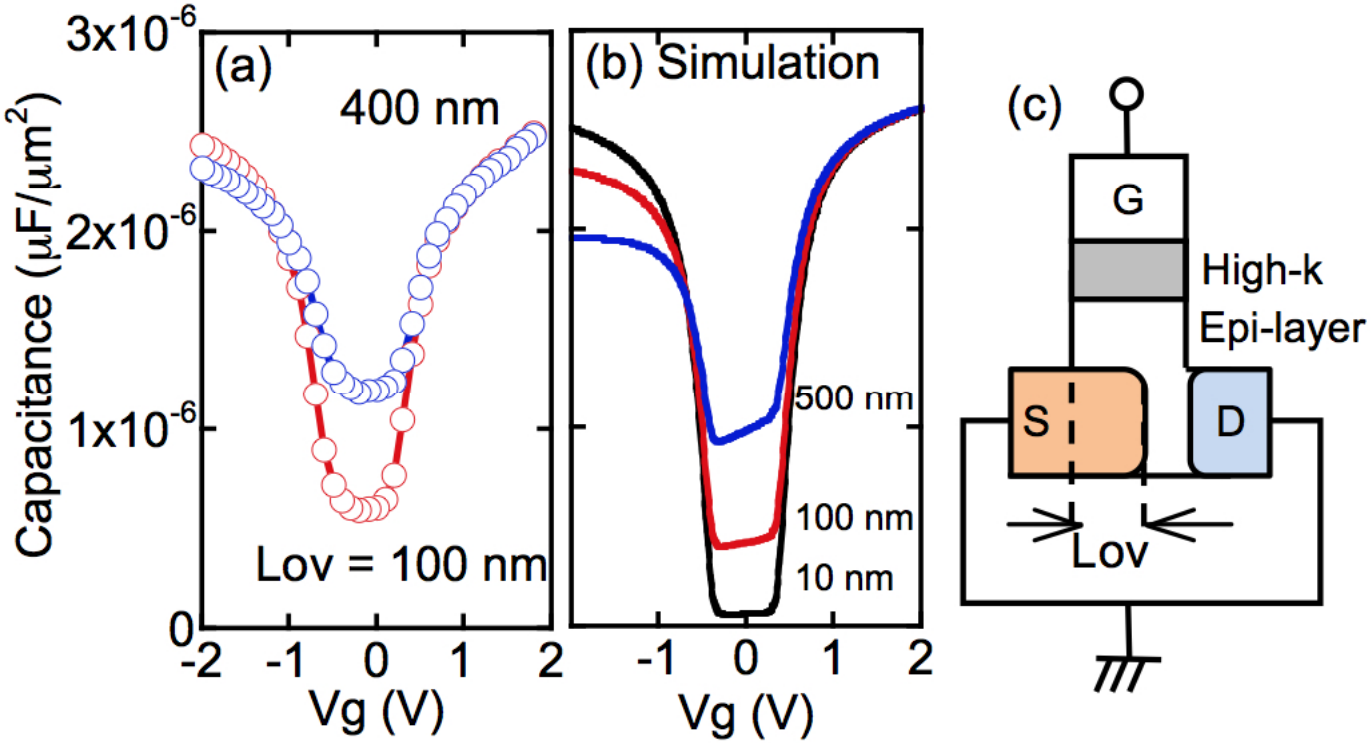
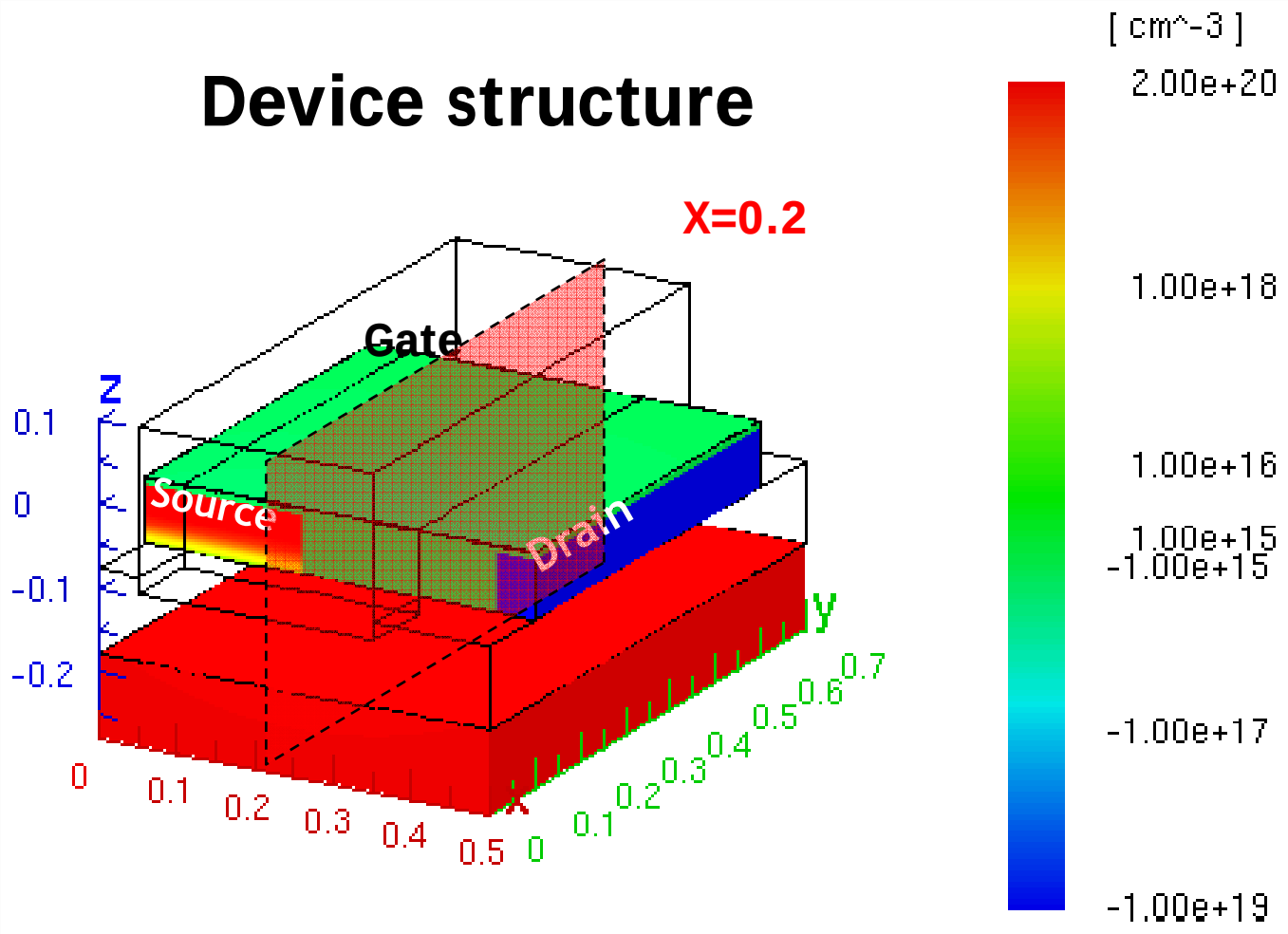


Fig. 4 Typical CV characteristics for the PP-capacitor of VTM TFETs. Variations in the different Lov are shown. (a) Experimental and (b) simulation results. (c) Measurement setup.

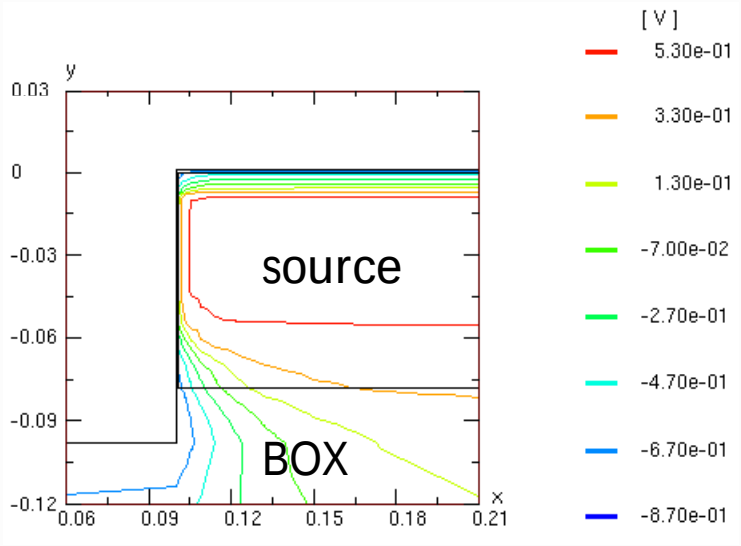
Device simulation of SE-TFET

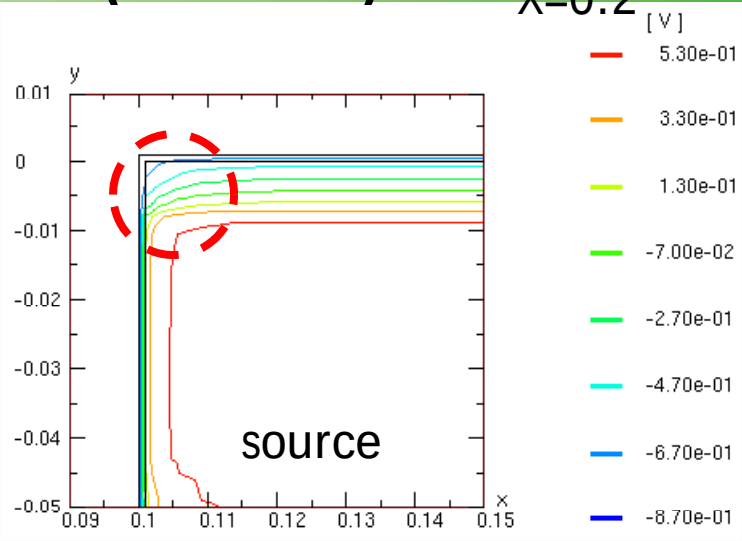


HyENEXSS™, v.5.5, Selete, 2011.

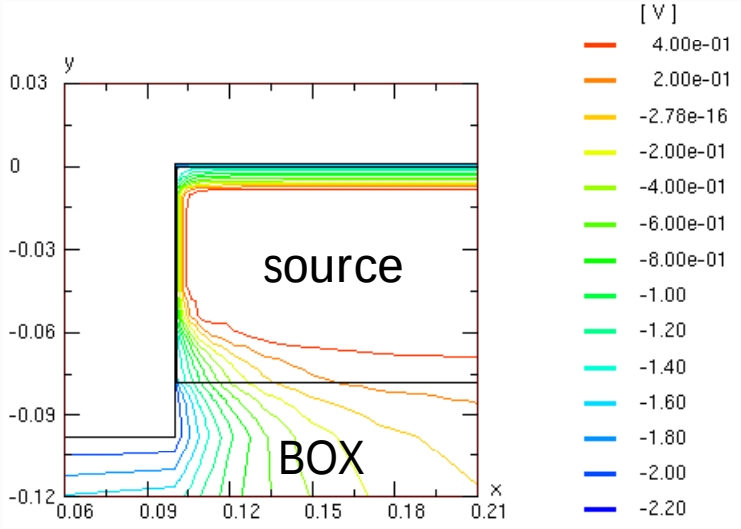
Sub-threshold condition (Potential)

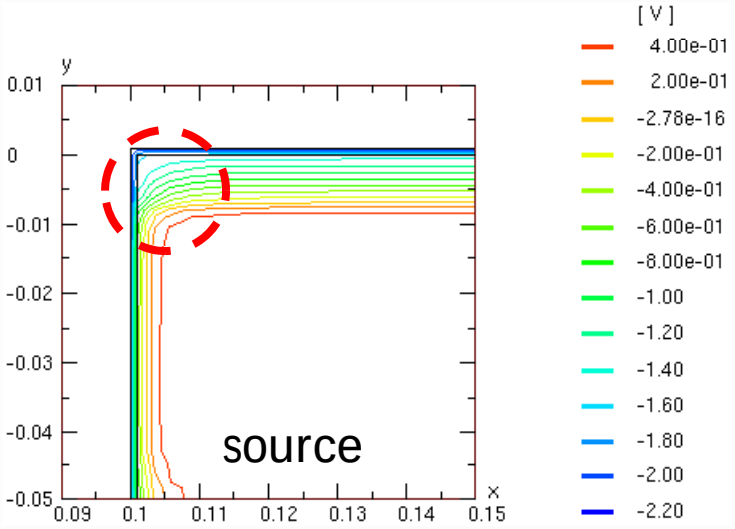
X=0.2





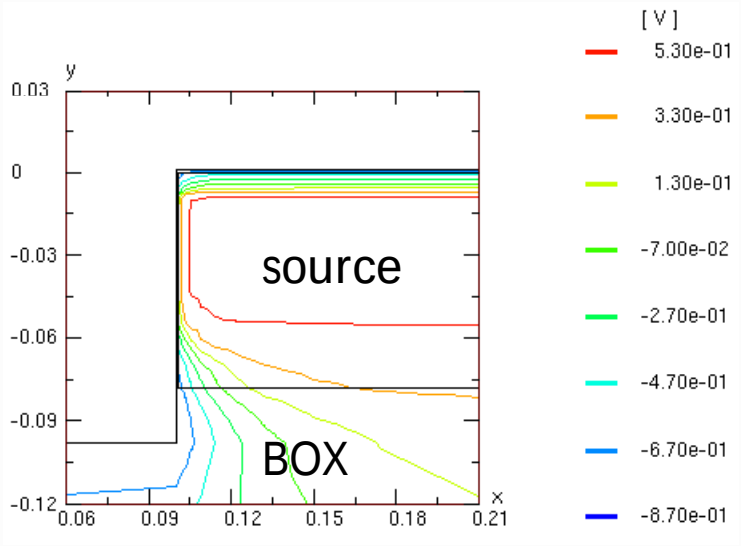
Saturation condition (Potential)

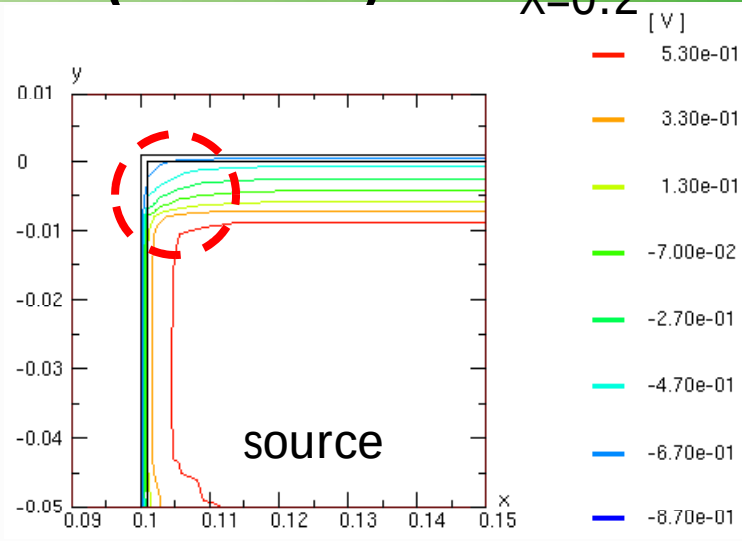




Sub-threshold condition (Potential)

X=0.2





Saturation condition (Potential)

Potential difference
> Si band gap
BTBT window opens at edge.