Mobility enhancement by integration of TmSiO IL in 0.65nm EOT high-k/metal gate MOSFETs

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Note to the reader

The following slides are a reduced version of the presentation delivered at ESSDERC 2013

Outline

- Introduction
  - EOT-mobility tradeoff
  - Advantages of high-k interfacial layers
- Device fabrication
  - TmSiO formation
  - Integration in a realistic gate stack
- Results
  - Electrical characterization of N- and P-MOSFETs
  - Mobility improvement compared to SiO_x/HfO_2 stacks
- Conclusion

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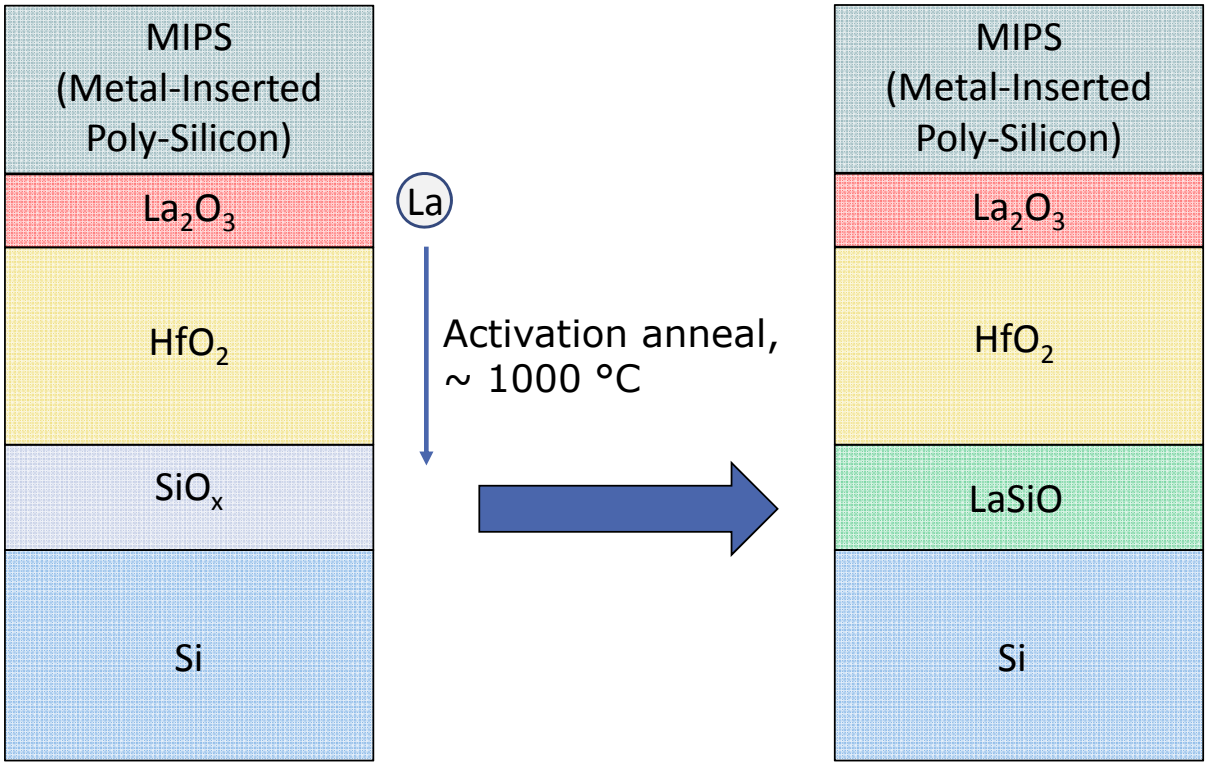
Introduction: IL scavenging

- High-k/metal gate technology suffers from EOT-mobility tradeoff
- The main factor is the thickness of the interfacial layer (IL)
- Scavenging is widely employed to control the IL thickness
- High field electron mobility has been shown to decrease by ~40cm^2/Vs per 0.1 nm reduction in IL thickness [Ando, Materials, 2012]

Introduction: LaSiO IL

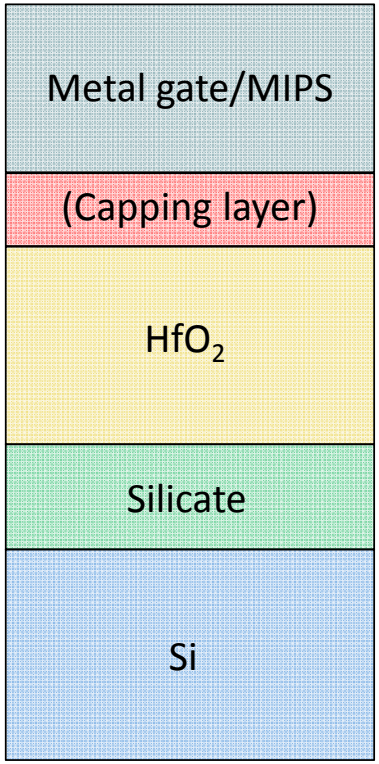
- IL thickness trade-off can be overcome by increasing κ
- La diffusion from capping layer can form a silicate IL with lower EOT



Compatible with:
- N-MOSFET
- Gate-first

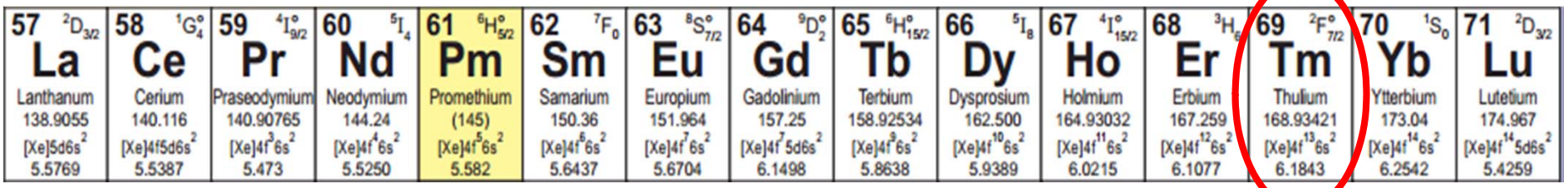
Introduction: high-k IL

- Direct integration of a high-k IL can be designed to achieve:
  - Compatibility with any gate stack (N and P)
  - Compatibility with gate-first and gate-last integration
  - Improvement of the EOT-mobility tradeoff curve
- The silicate should be chosen as to provide:
  - High κ (>10)
  - Good electrical quality of the interface with Si
  - Compatibility with Hf-based gate stacks



Introduction: TmSiO

- Silicates can be formed from many lanthanide oxides



- Requirements:
  - Low reactivity with Si and H_2O -> High atomic number
  - k of the oxide > 15
  - E_G of the oxide > 5 eV
  - Conduction and valence band offsets > 1 eV
- Tm_2O_3 is a good candidate: k=16, E_G=5.5 eV, CBO/VBO >2eV [Wang 2012]
- TmSiO has similar dielectric constant to LaSiO (k=10-12)
- TmSiO IL has been shown to provide good electrical properties [Dentoni Litta et al., IEEE Trans. Electr. Dev., 2013]

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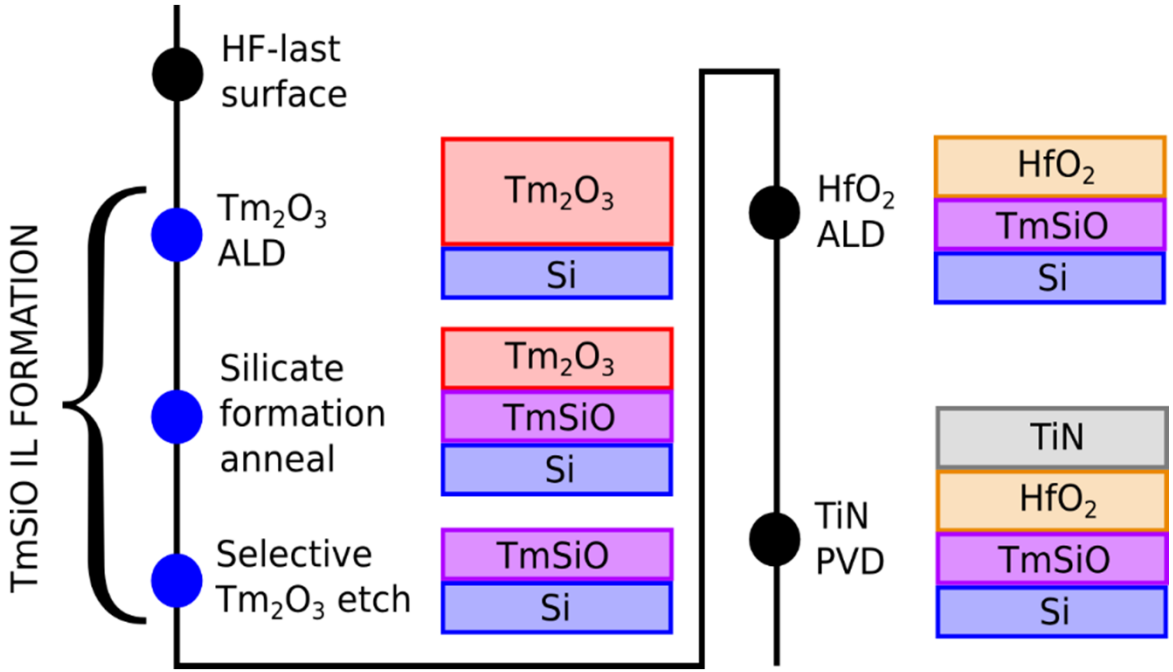
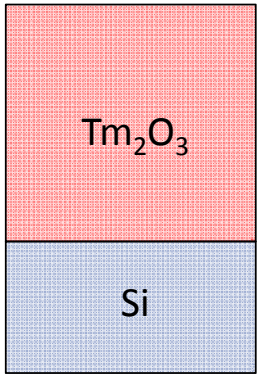
Device fabrication

- Thulium silicate IL module is integrated with HfO_2/TiN stack
- Gate-last CMOS process



Device fabrication

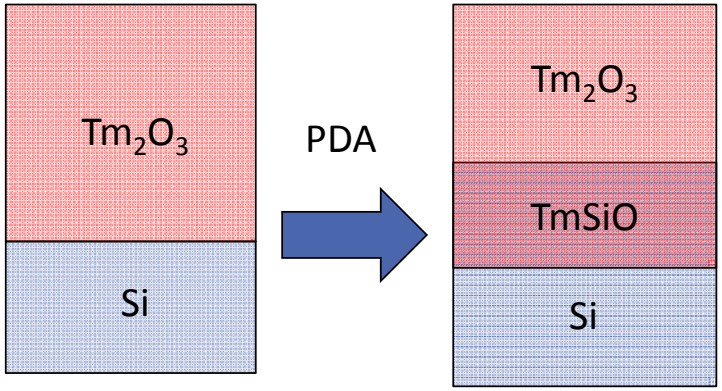
- Starting substrate with pre-formed source/drain
- Surface clean in H_2SO_4:H_2O_2 and 5% HF
- Deposition of Tm_2O_3 by ALD

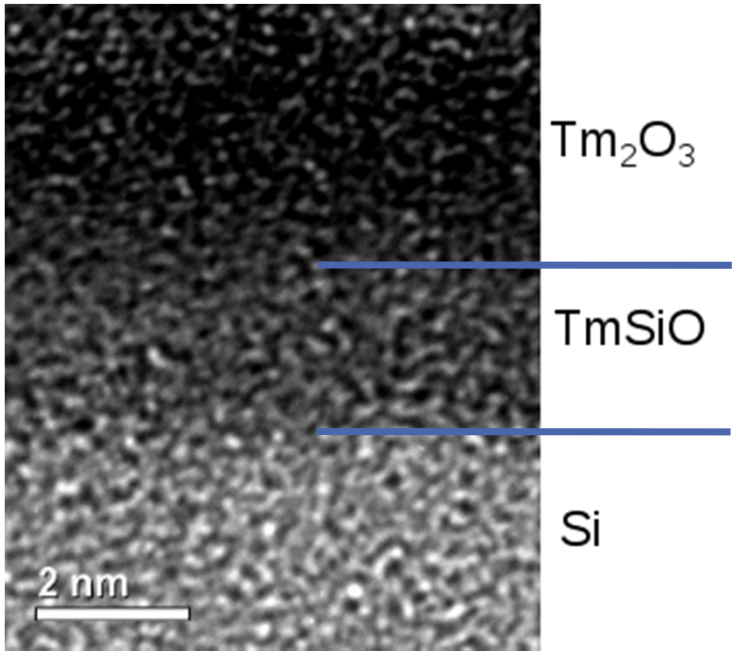


- System:
  - Beneq TFS 200
- Precursors:
  - $TmCp_3$ and H_2O
- Deposition temperature:
  - 250 °C

Device fabrication

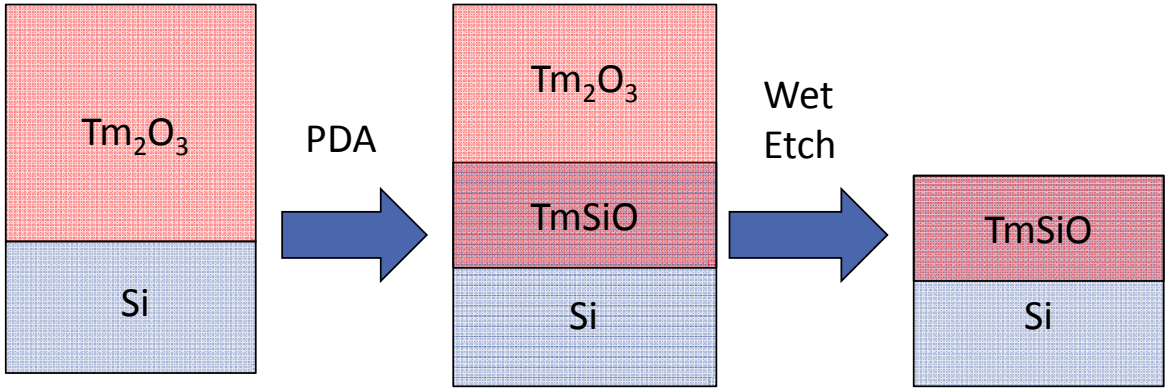
- Post deposition anneal in N_2 for 60s
- TmSiO thickness is controlled by PDA temperature [Dentoni Litta et al., ULIS 2013]
- PDA at 500 °C yields 0.8±0.1 nm





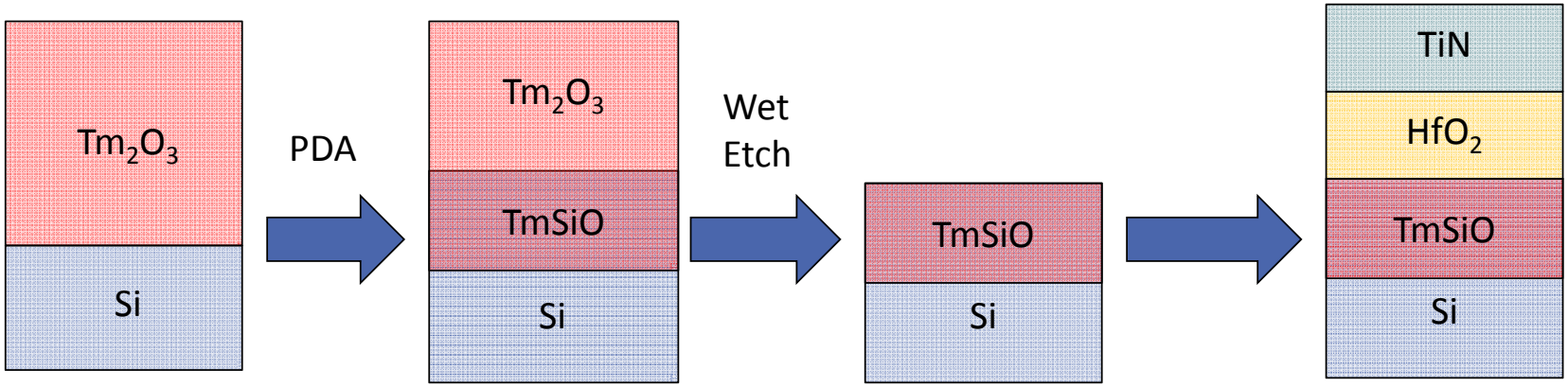
Device fabrication

- Tm_2O_3 needs to be removed selectively
- Etching solution needs to be CMOS-compatible
- H_2SO_4 etches Tm_2O_3 with > 23:1 selectivity toward TmSiO

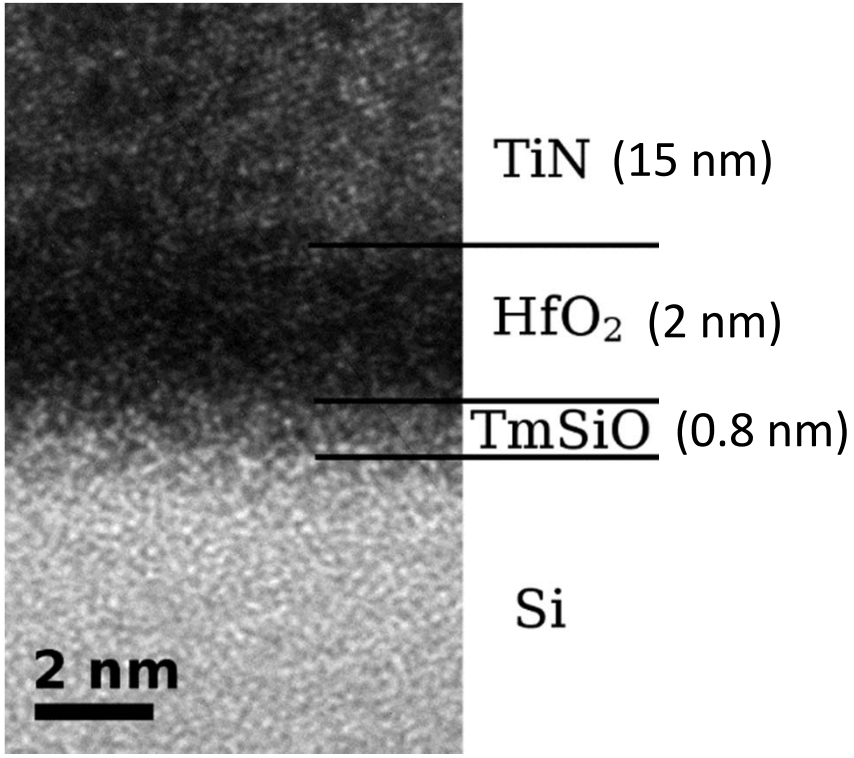


Device fabrication

- Deposition of HfO_2 by ALD (2 nm)
- Deposition of TiN by reactive sputtering (15 nm)
- Post metallization anneal (N_2, 425 °C, 5 min)



Device fabrication



- Gate patterning
- PECVD SiO_2 passivation
- Ti/TiW/Al metallization
- Forming gas anneal

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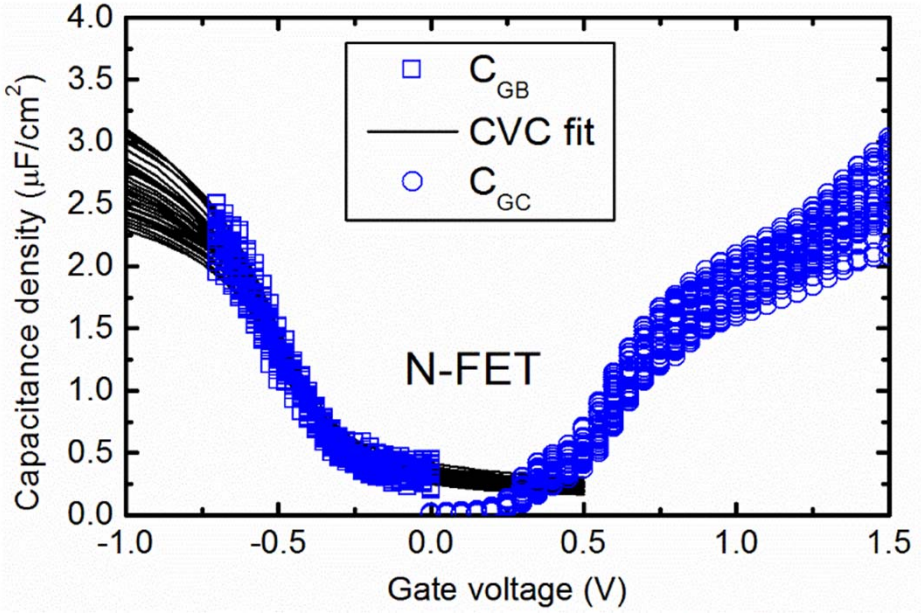
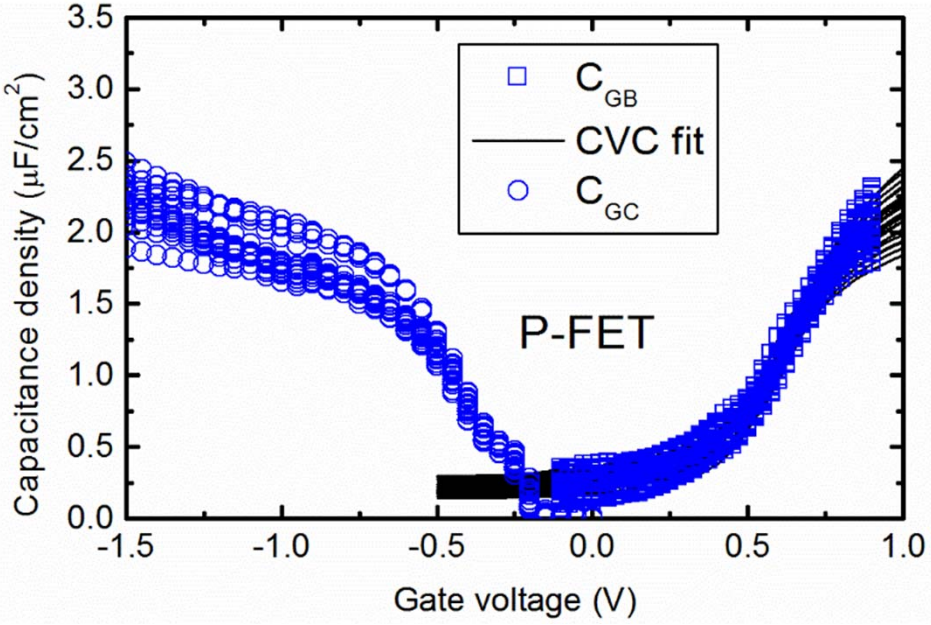
Results: C-V characterization



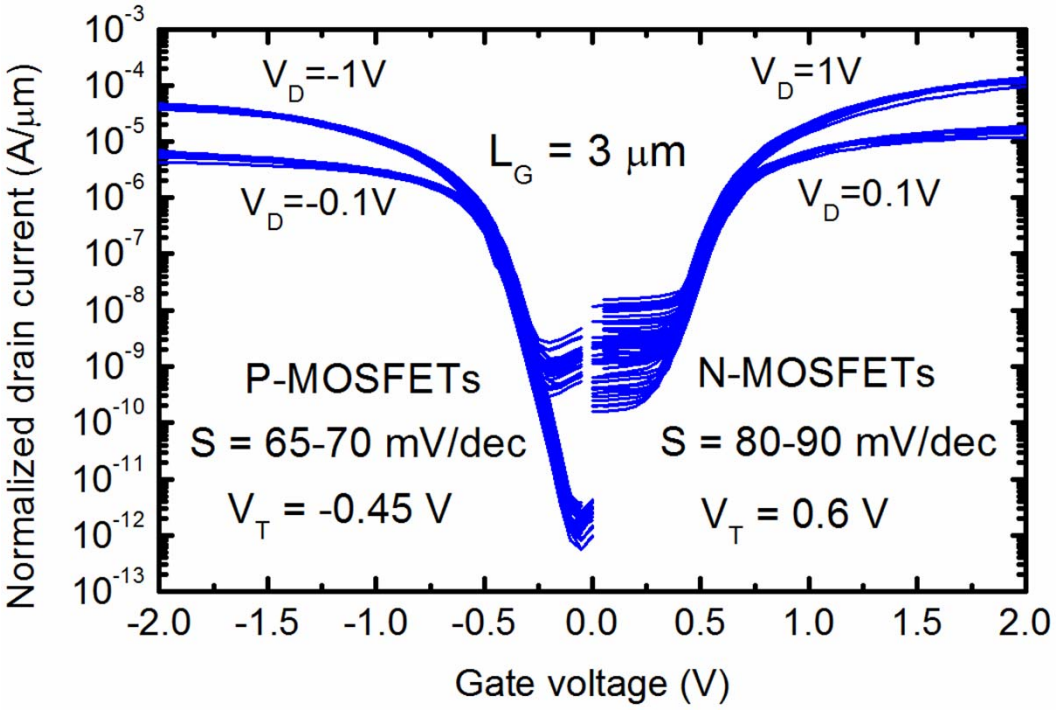


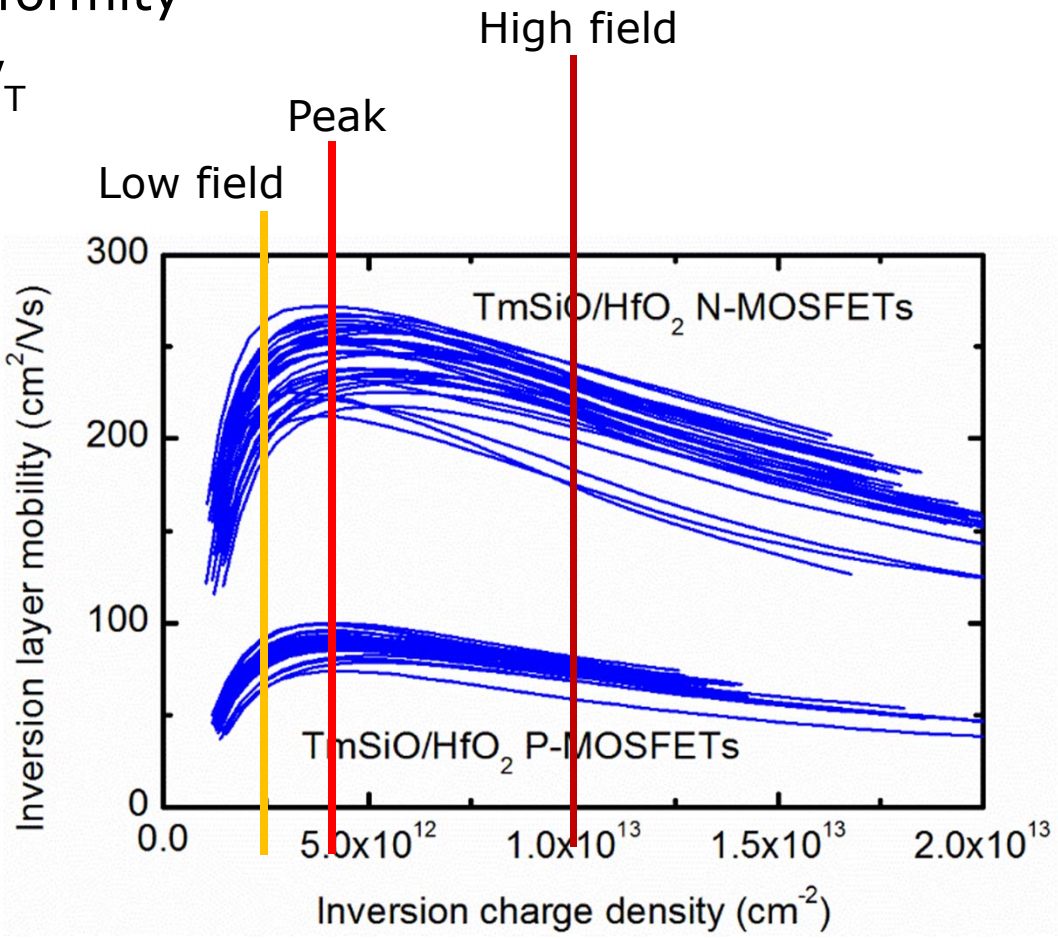
- 30 N-FETs and 30 P-FETs measured on 100 mm wafer
- Low hysteresis:
  N: 0-50 mV, P:0-20 mV

- EOT extracted by CVC fitting [Hauser 1998]:
  N: 0.65-1.1 nm P: 0.8-1.2 nm
- Perfect agreement with CET values:
  N: 1.0-1.6 nm P: 1.25-1.6 nm

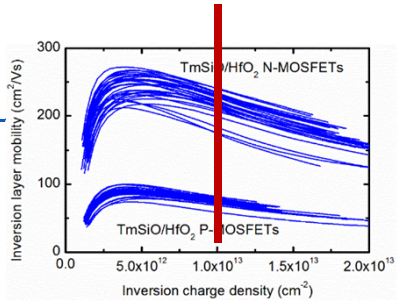
Results: I-V characterization

- $I_D V_G$ characterization shows good uniformity
- Low subthreshold slope, symmetric V_T
- Mobility extracted by split-CV

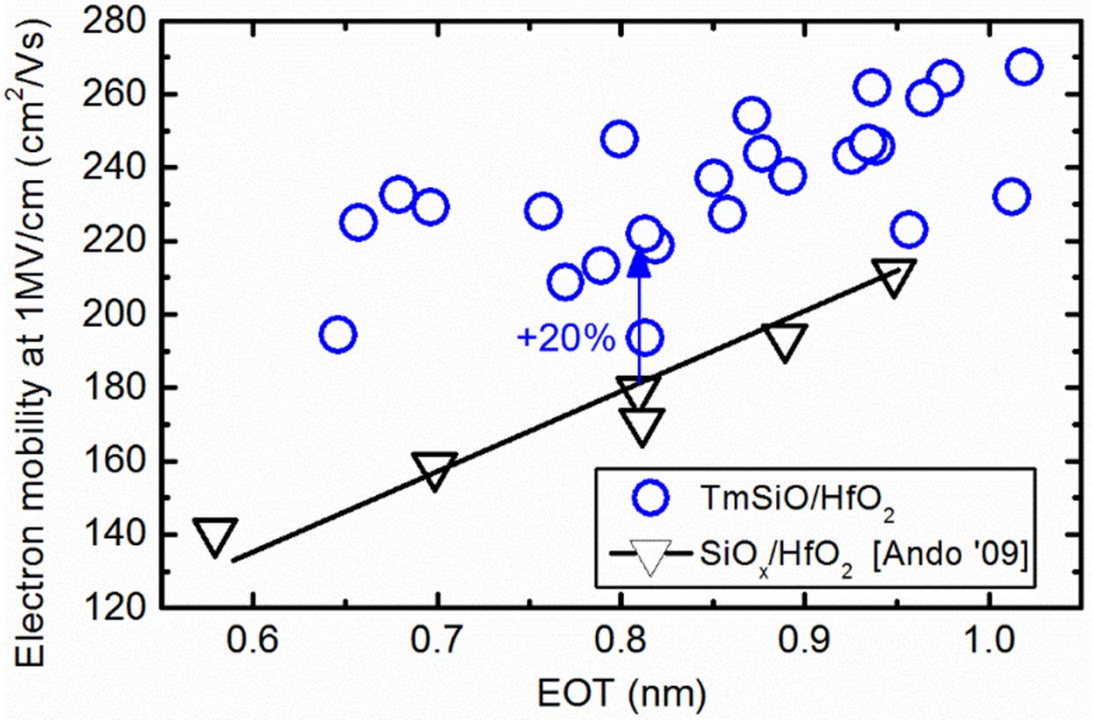


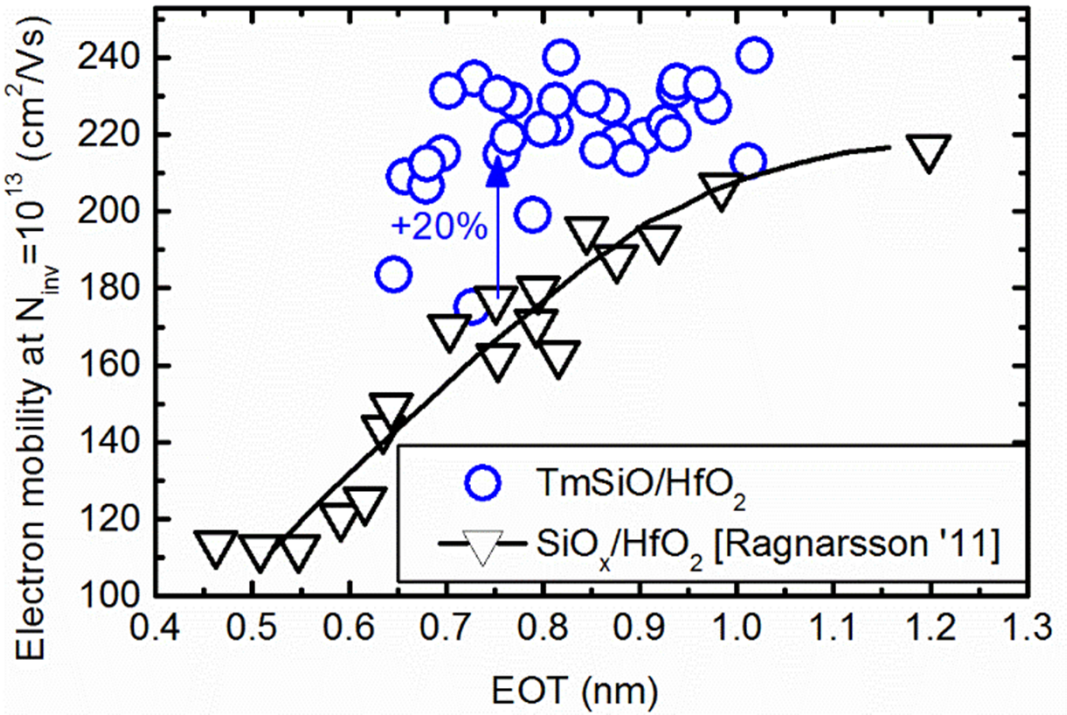


Results: high-field electron mobility



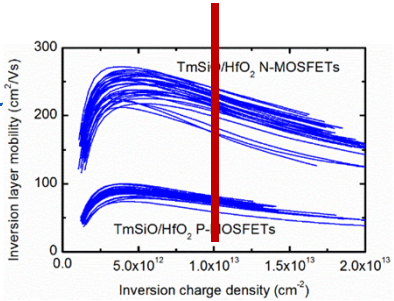
- Mobility improvement compared to SiO_x/HfO_2 stacks
- 20% enhancement for N-MOSFETs at high field

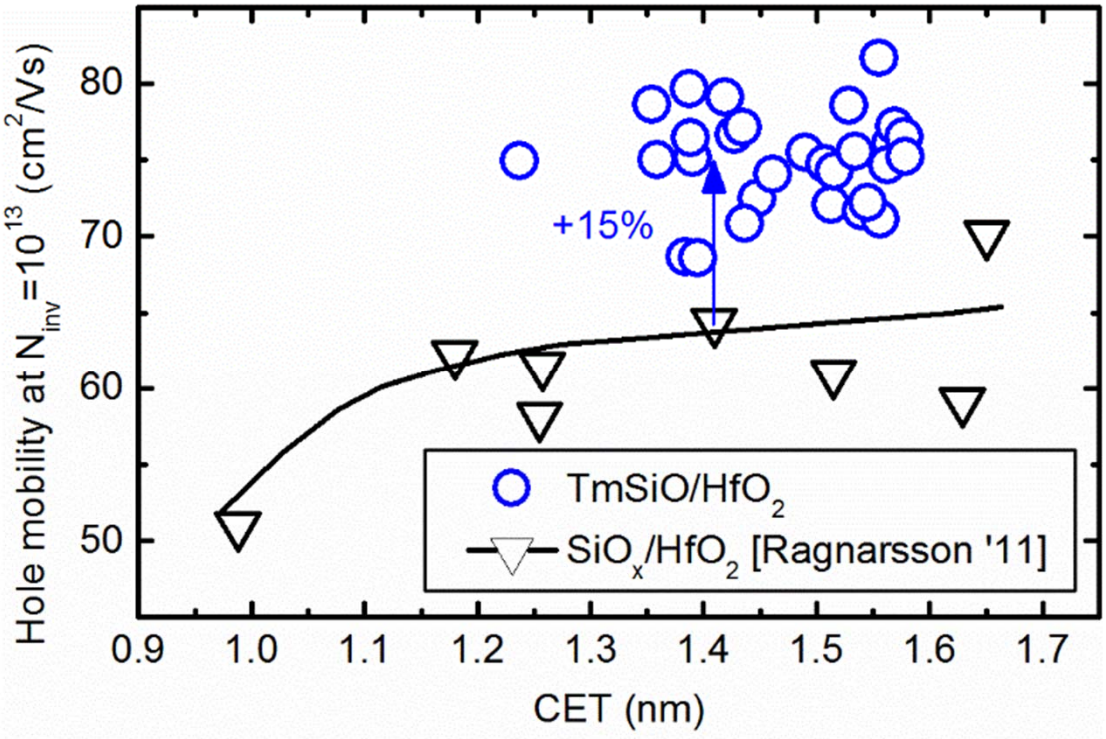




Results: high-field hole mobility

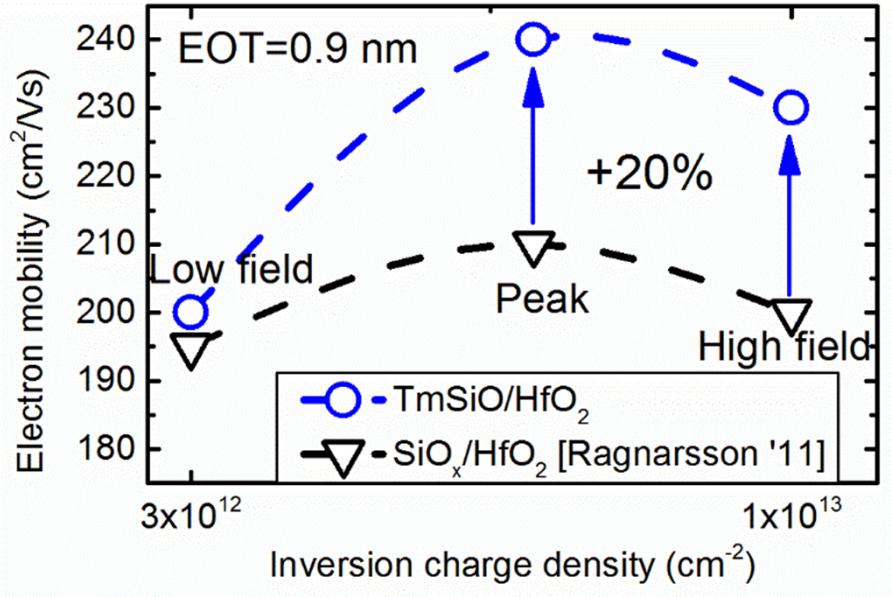
- Mobility improvement compared to SiO_x/HfO_2 stacks
- 15% enhancement for P-MOSFETs at high field





Results: interpretation of the N mobility data

- Remote scattering mechanisms are modulated by IL thickness
  - Thicker TmSiO IL (~0.8 nm) can reduce remote scattering from HfO_2
- Electron mobility in $TmSiO/HfO_2$ versus reference SiO_x/HfO_2:
  - Comparable low-field mobility
  - 20% higher peak and high-field mobility



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Conclusion

- TmSiO IL can be integrated in HfO_2-based gate stacks
- Good electrical performance achieved for both N and P-MOSFETs

  Subthreshold slope = 80-90 mV/dec for NFETs, 65-70 mV/dec for PFETs
- Low EOT achieved in gate-last CMOS process

  0.65 nm for NFETs, 0.8 nm for PFETs
- Observed electron/hole mobility improvement at high field

  +20% for NFETs, +15% for PFETs

  Likely consequence of the higher physical thickness of the IL

Acknowledgment

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Thank you for your attention