Novel Back-Biased UTBB Lateral SCR for FDSOI ESD Protections

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Outline

- **Introduction & Context**

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- **Lateral Silicon Controlled Rectifier (LSCR) Fabrication & Principle**

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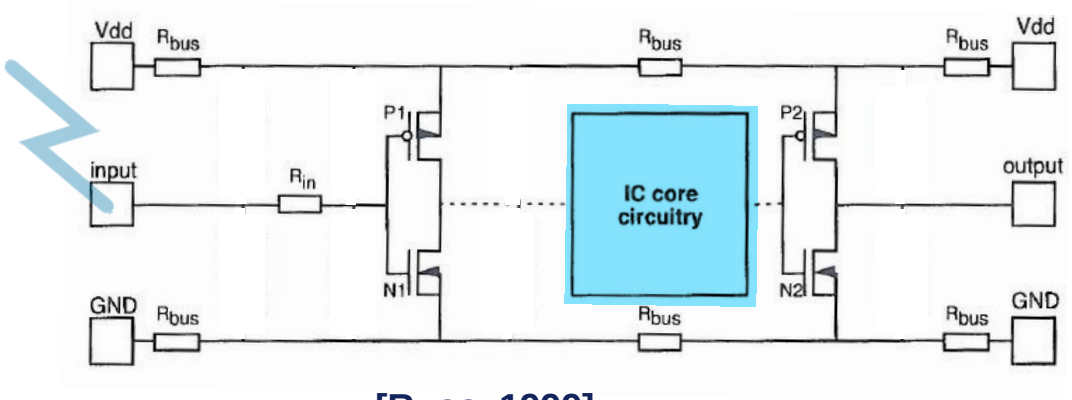
- **LSCR Experimental Results**
- **Conclusions**

Introduction & Context

Introduction & Context (1)

- **Electro-Static Discharge Damages**



[Russ, 1999]

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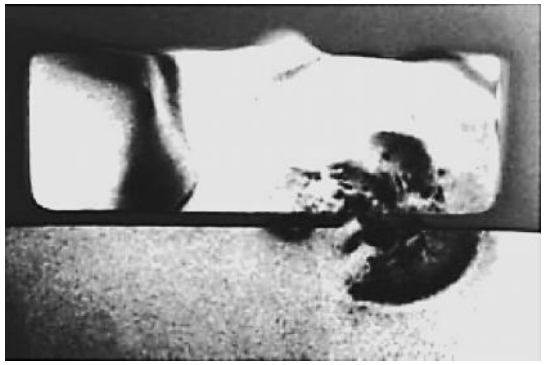
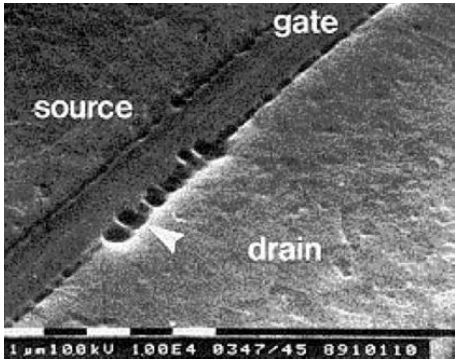
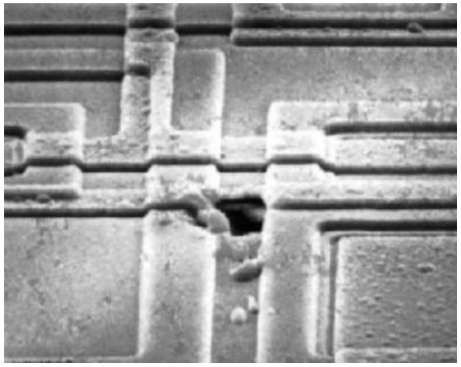


Gate oxyde breakdown

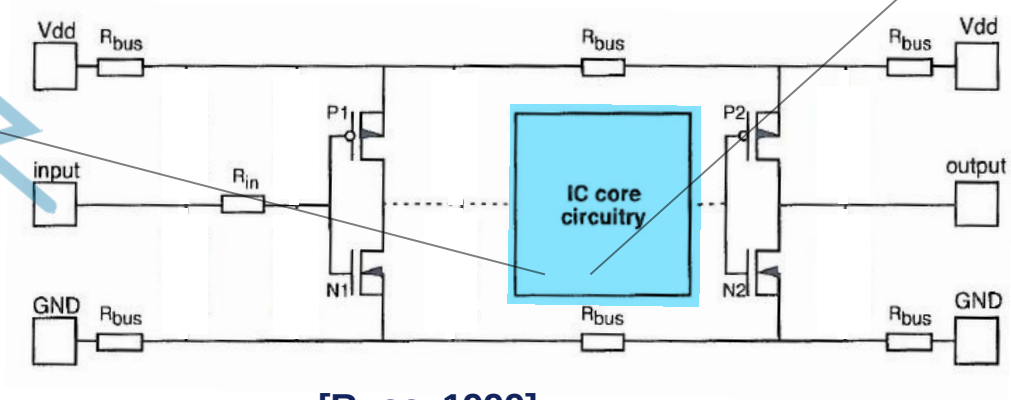


Drain junction filamentation



Interconnects damages

[Semenov, O., 1999]



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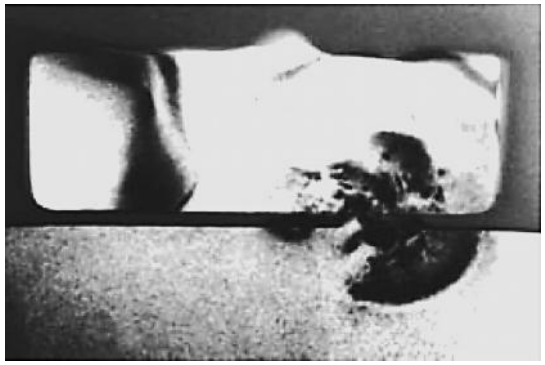

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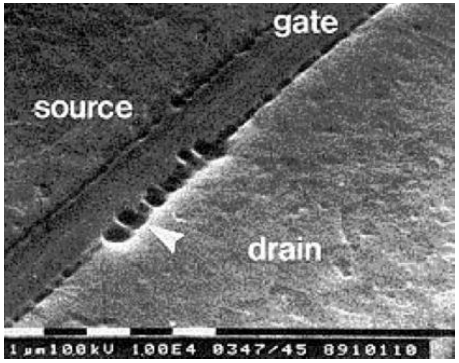

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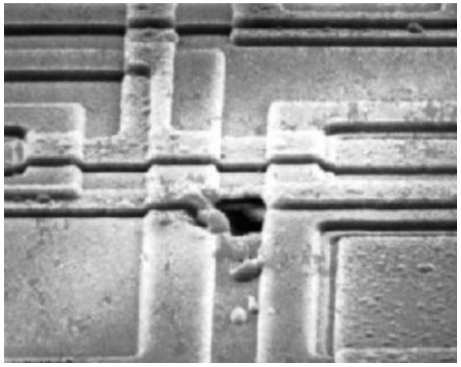

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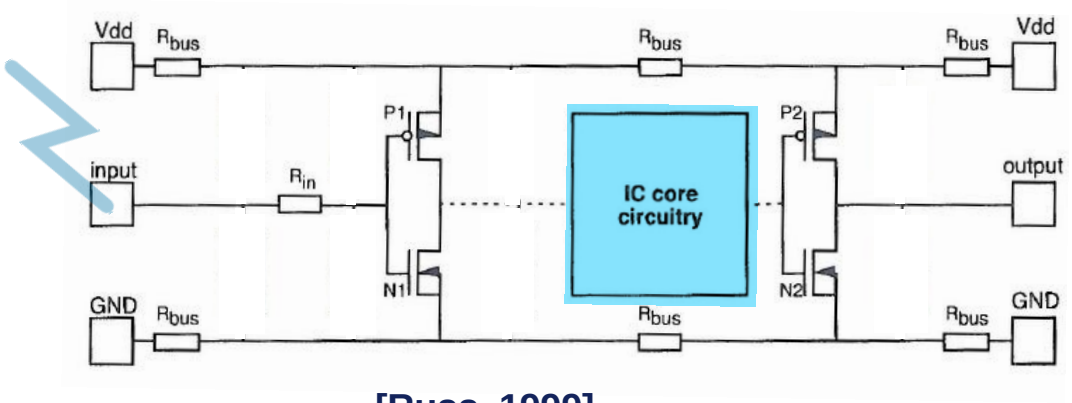
ESDs are destructive events



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Introduction & Context (1)

- **Electro-Static Discharge Protection Requirements**
  - **Principle & Design of a protection**
    - **“Robustness, Effectiveness, Speed, Transparency”**
      [Amerasekera & Duvvury 2002]
  - $Z_{CLAMP} << Z_{CORE}$
    - **under ESD condition**
  - $Z_{CORE} << Z_{CLAMP}$
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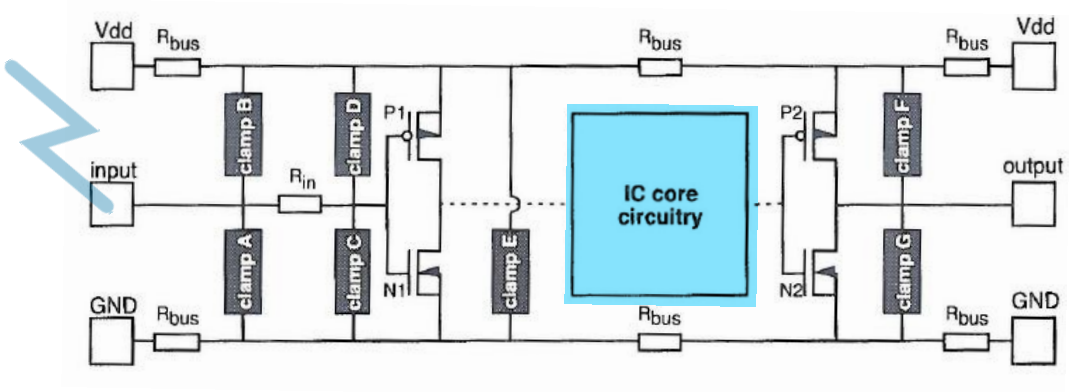

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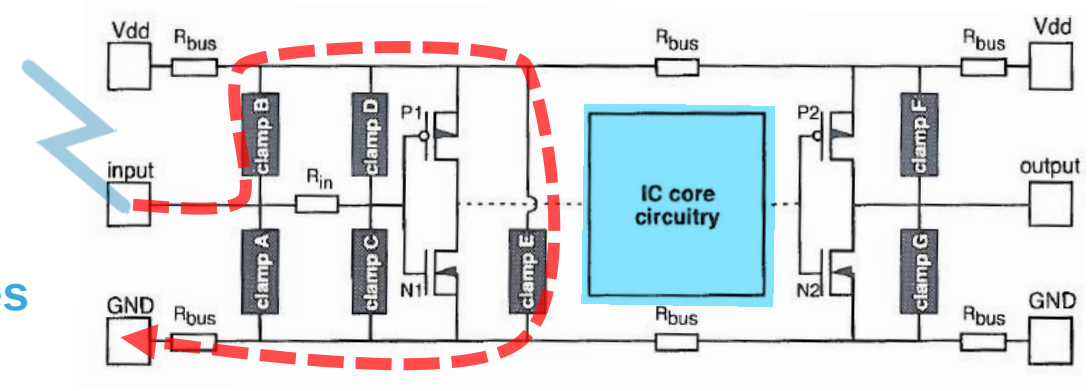

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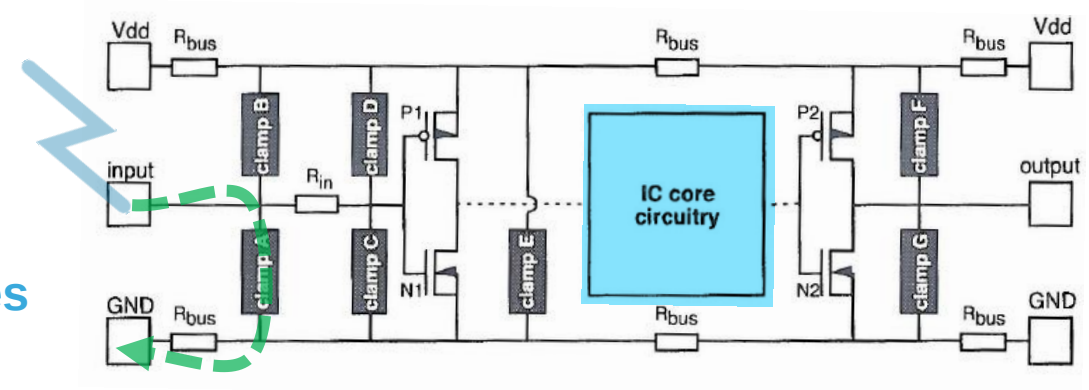

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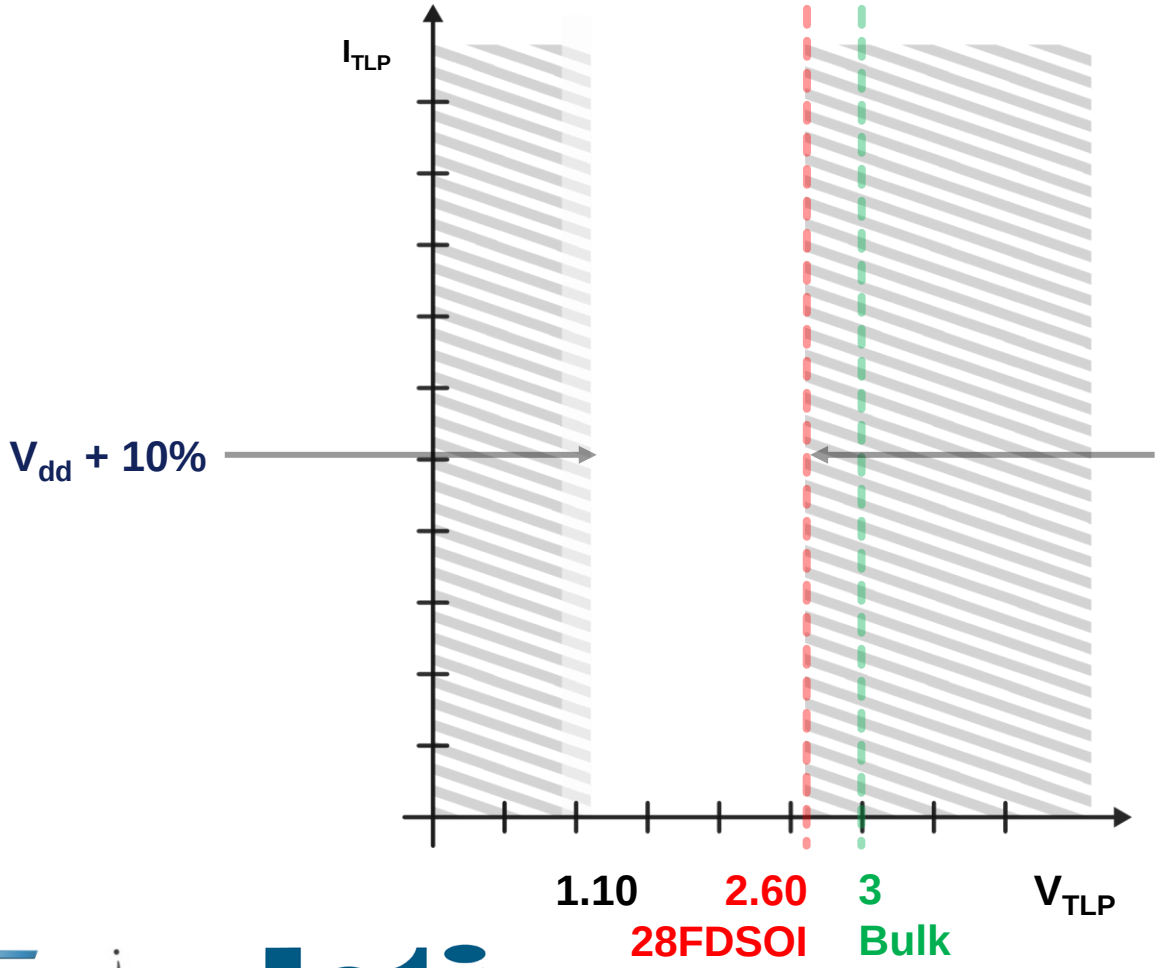
Introduction & Context (2)

- **Reduced ESD design window in Fully Depleted SOI**



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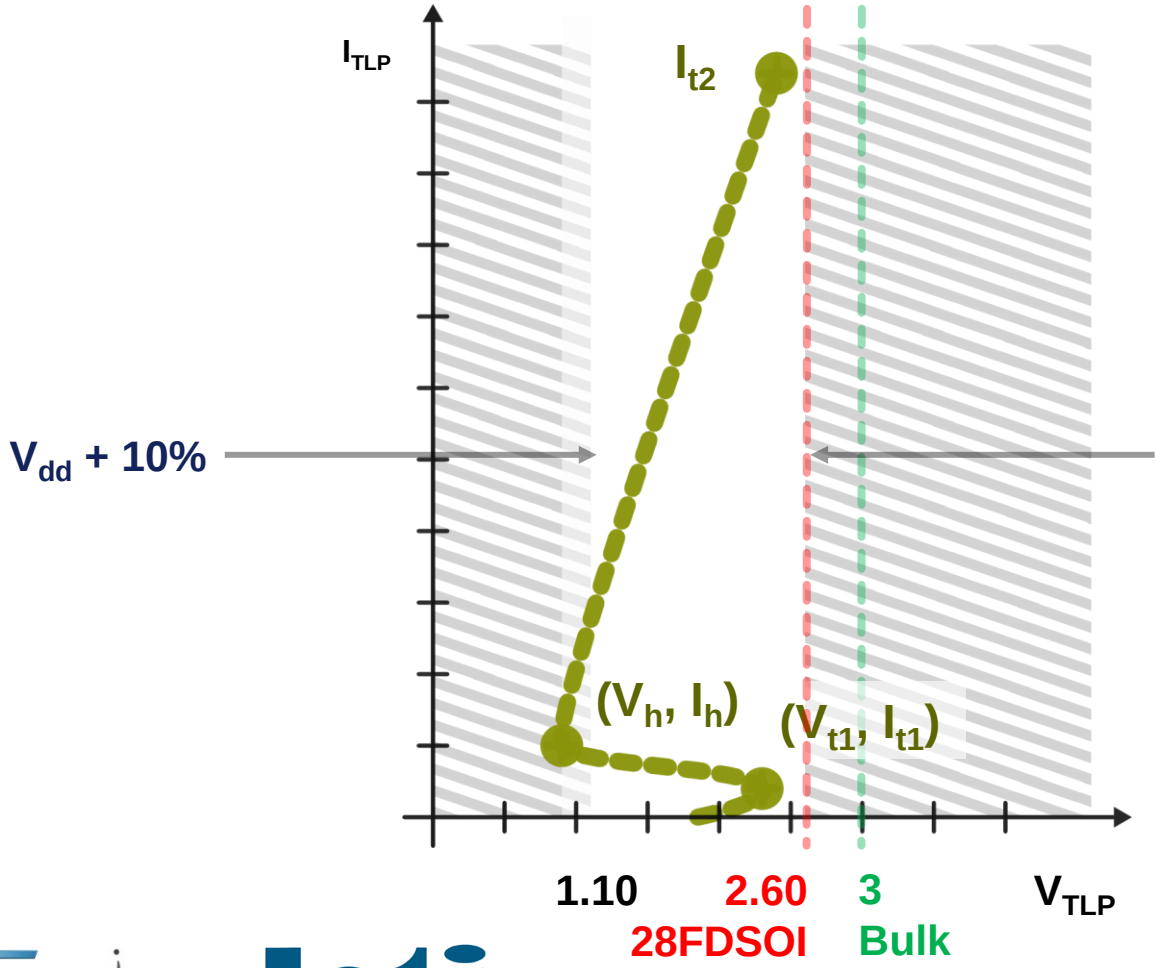

I_{t2} : Failure current
V_h : Holding voltage
V_{t1} : Triggering voltage

« Core MOS » breakdown
[Benoist et al. 2011]

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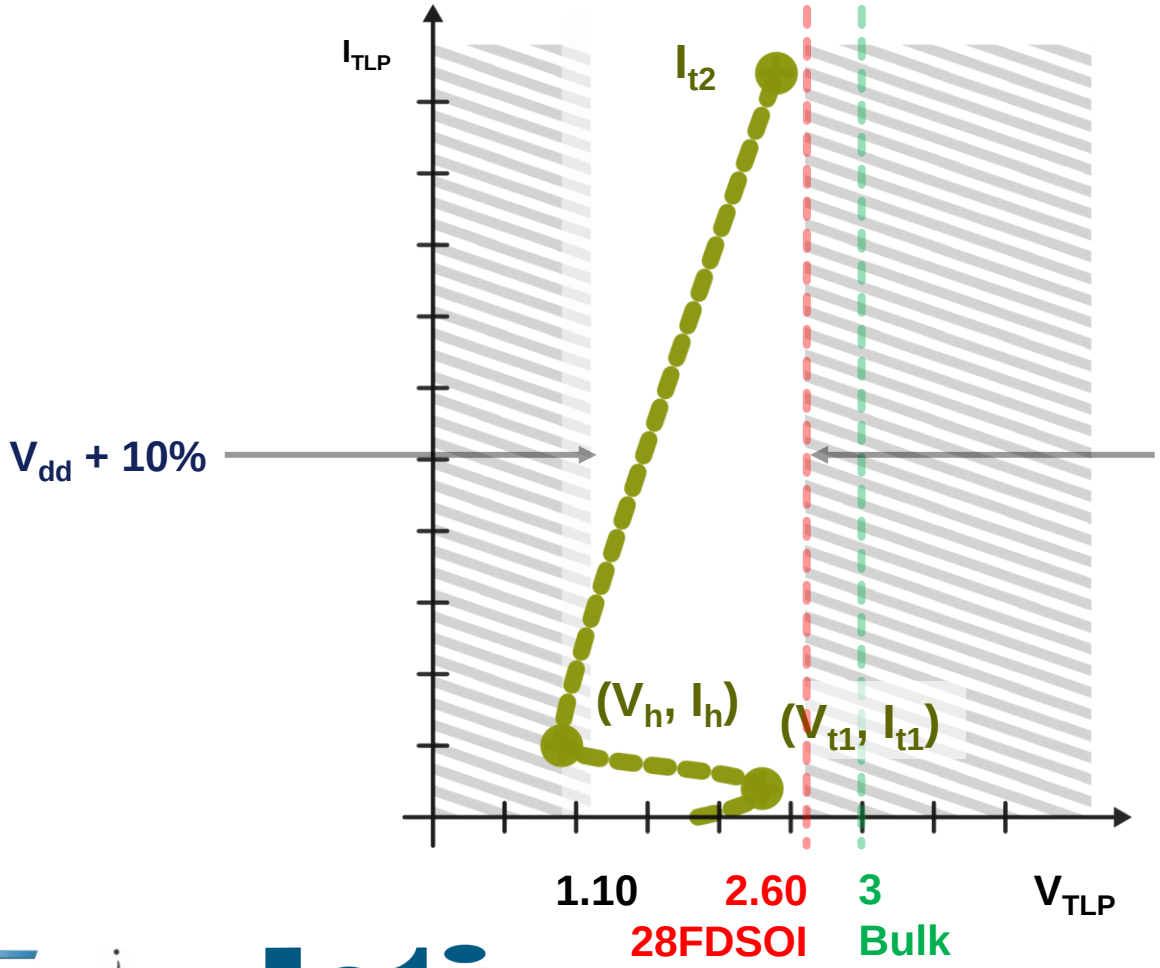

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→ new candidate for FDSOI ESD protection : LSCR

LSCR Fabrication & Principle

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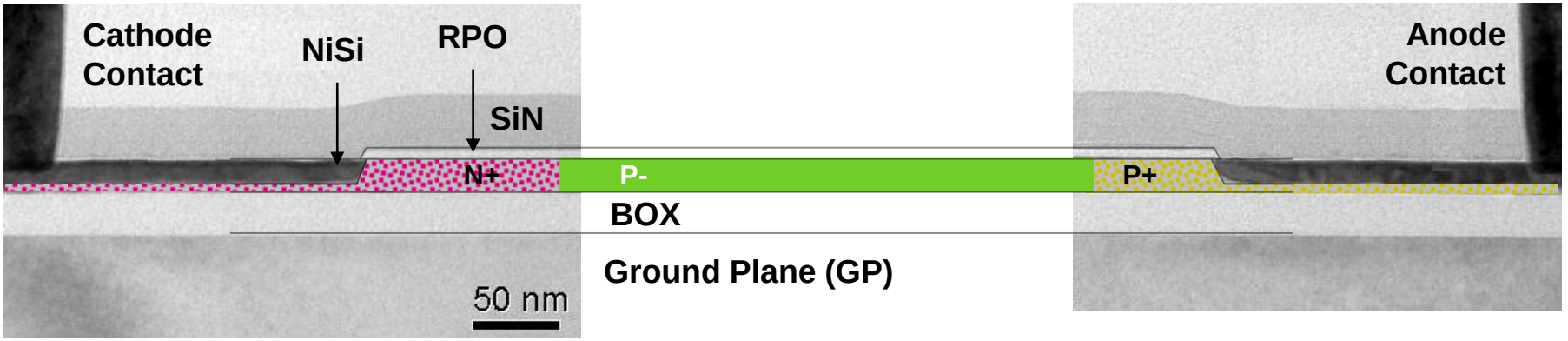
LSCR Fabrication & Principle

- **Device Geometry**
  - **From SOI PIN-Diode…**



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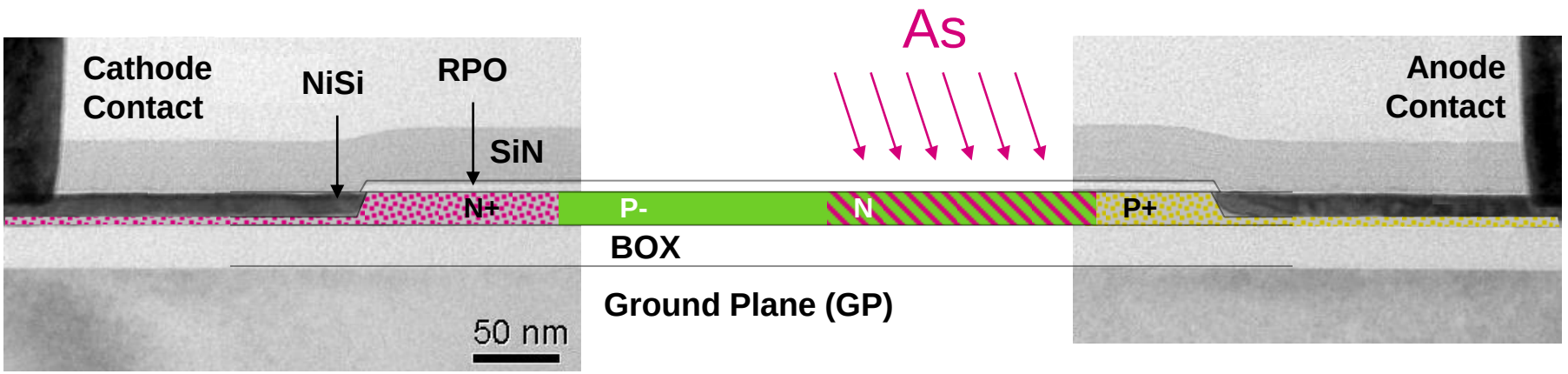

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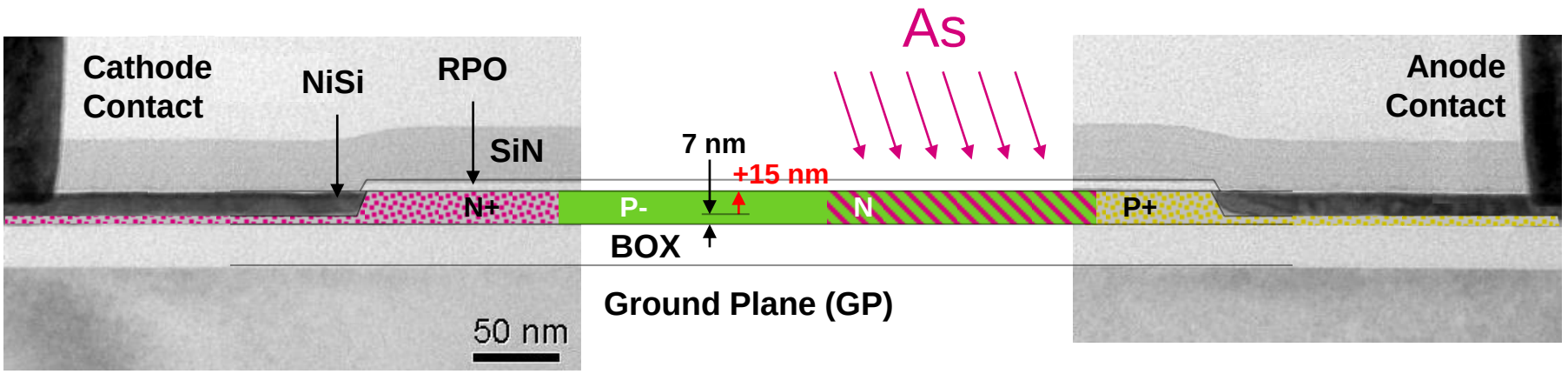
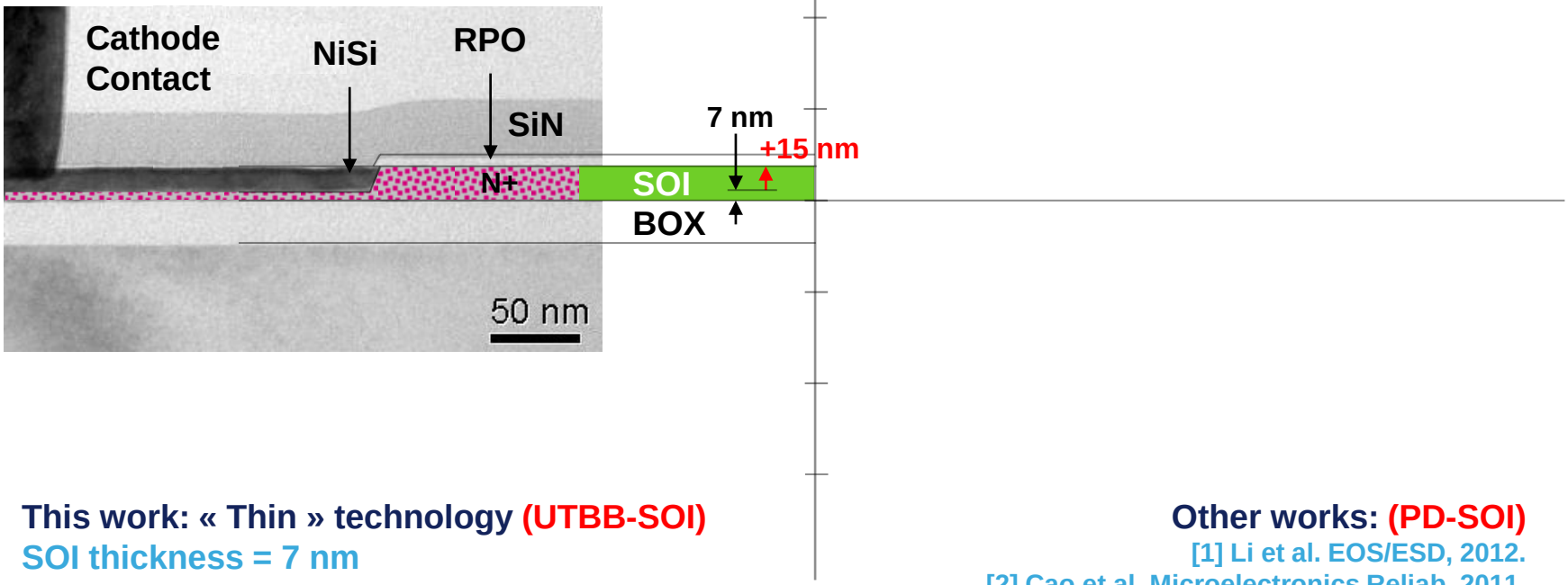


- Lateral N+/P/N/P+ arrangement
- SOI thickness = 7 nm
- BOX = 25 nm
- No Front Gate deposited [1]
- Si. Epitaxy (+15 nm) on whole structure (raised Source/Drain)

LSCR Fabrication & Principle

- **Device Geometry**



This work: « Thin » technology (UTBB-SOI)
SOI thickness = 7 nm
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Other works: (PD-SOI)
[1] Li et al. EOS/ESD, 2012.
[2] Cao et al. Microelectronics Reliab, 2011.
[3] Marichal et al. EOS/ESD 2005.
[4] Entringer et al. EOS/ESD 2006.

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LSCR Fabrication & Principle

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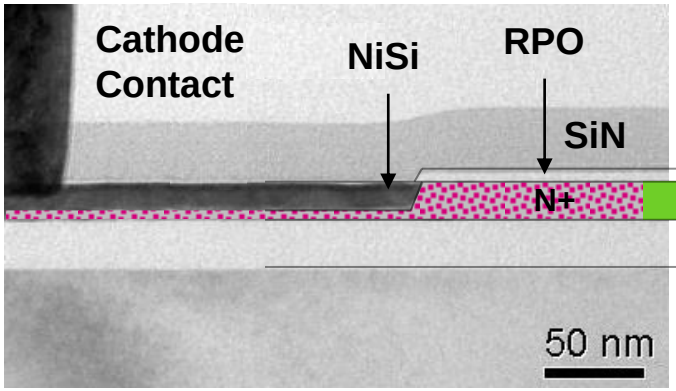

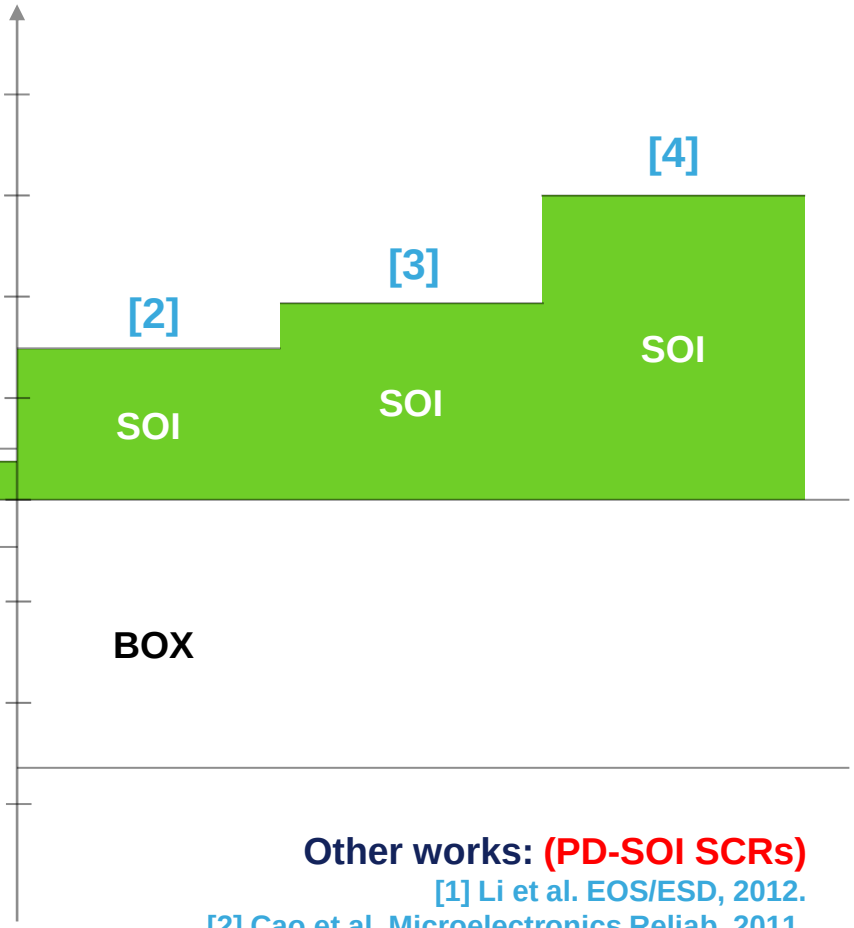

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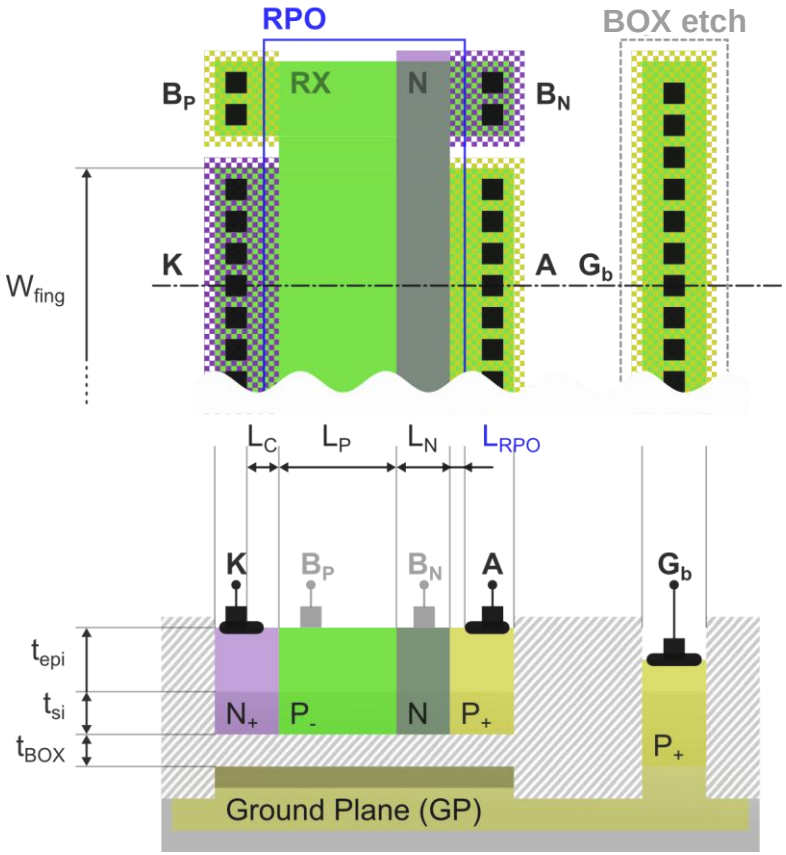
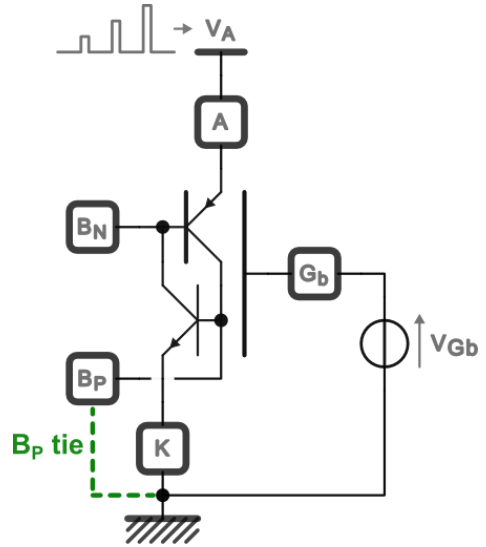
LSCR Fabrication & Principle

- **Device Geometry**
  - **« Side Base Contacts »:**
    - P-Base (B_P) can be tied to K (« locked » mode)
    - N-Base (B_N) left floating in this study
  - **Ground-Plane (GP) used as a back gate**

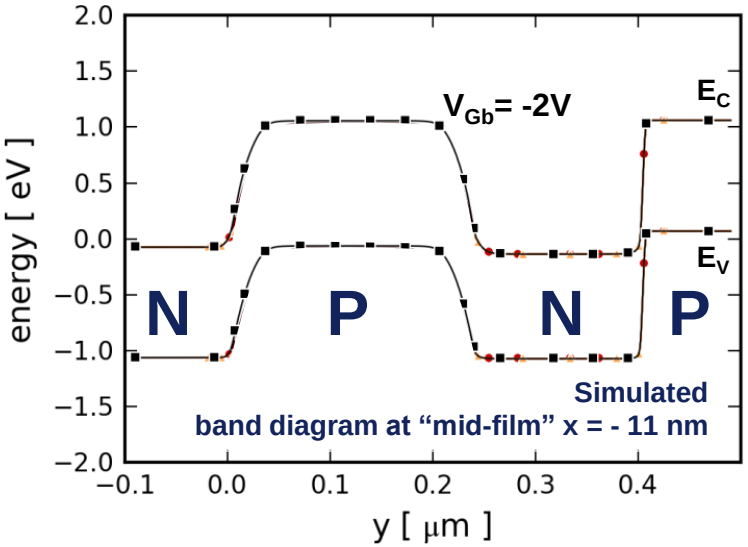


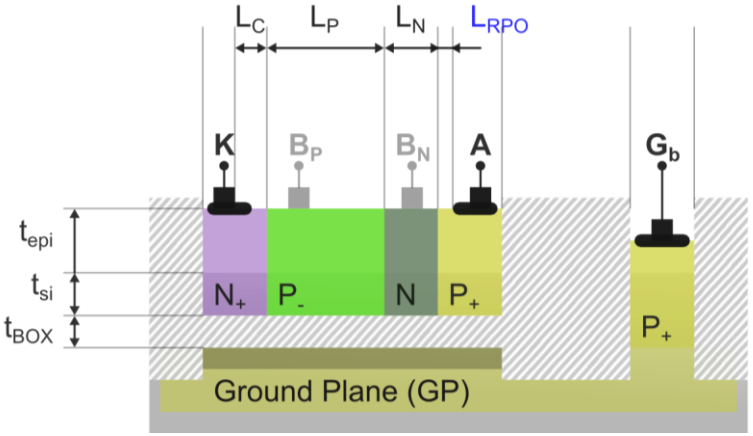
LSCR Principle

- **NPN Modulation**
  - NPNP = Thyristor = Two inter-linked BJTs [1,2] with shared **BC junctions**



[1] Moll et al., Proceedings of the IRE, 1956.
[2] Sze, Wiley, 1981.





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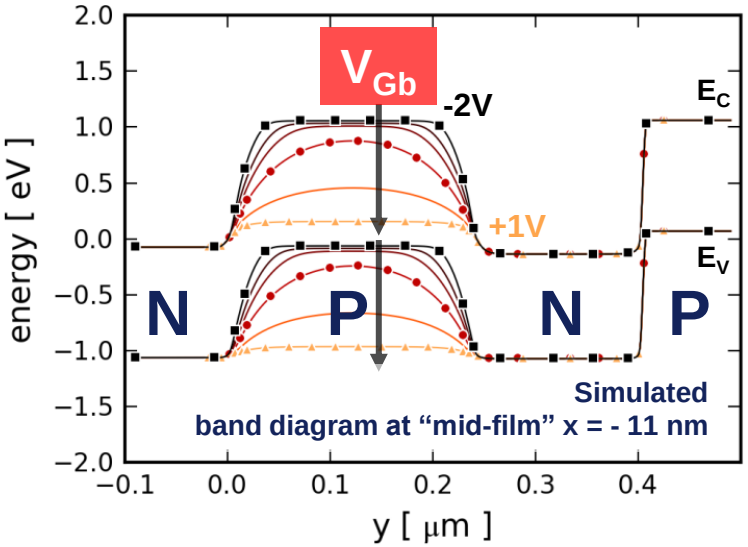
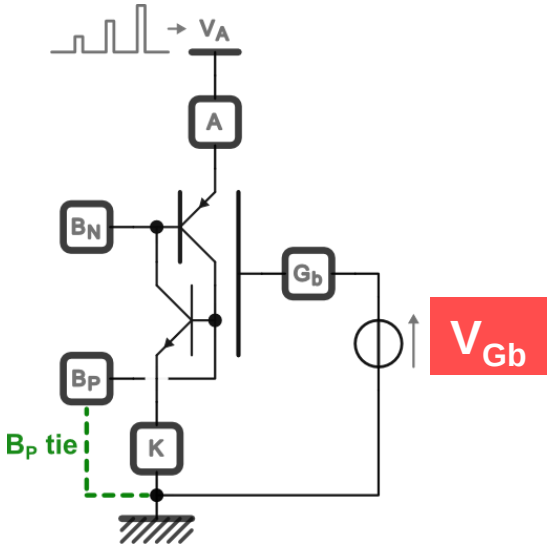
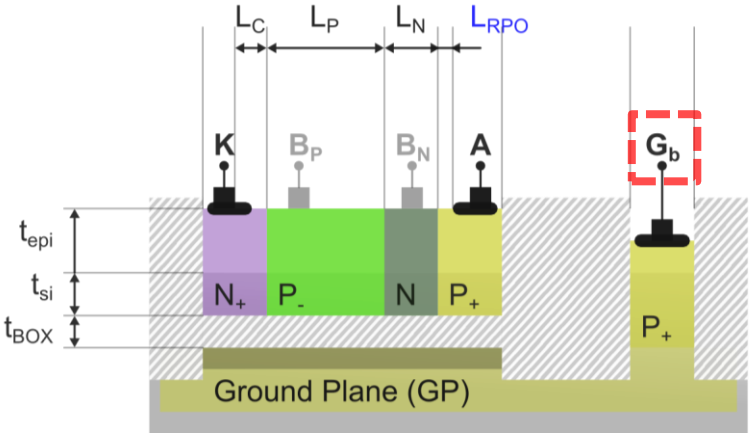




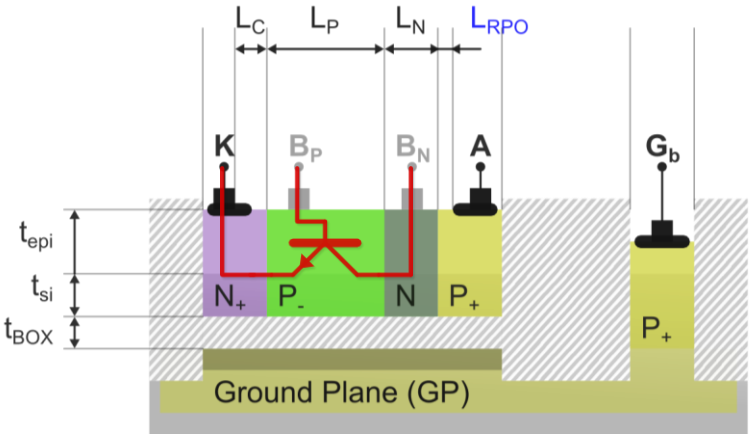


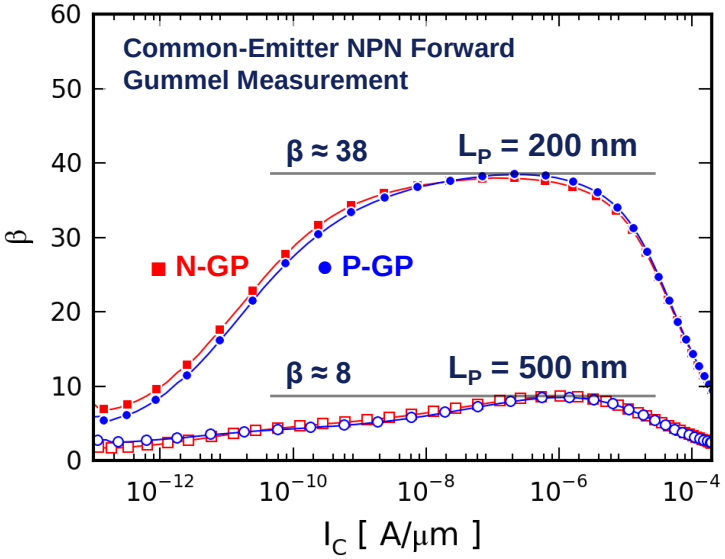
LSCR Experimental Results

Experimental Results

- **NPN Characterization**

  - NPN gain known to impact the SCR behavior (V_{t1}, I_{t1}, I_{leak}…)
  - ‘Strong’ accumulation condition in the NPN base : V_{Gb} = -2V
  - Common-Emitter Gain β (= I_C/I_B) mainly depends on NPN Base length: L_P





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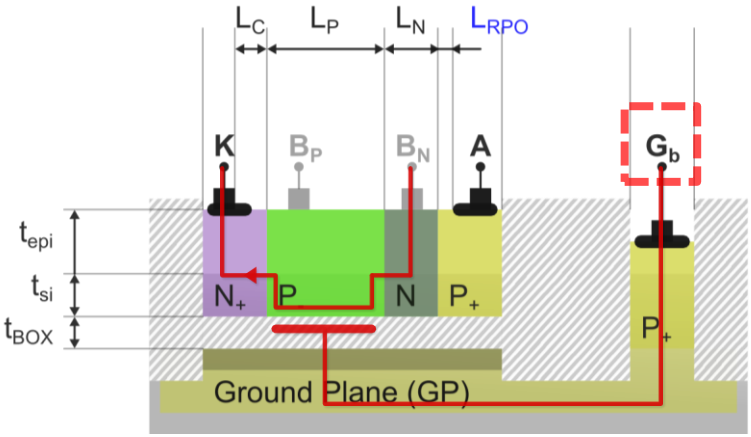

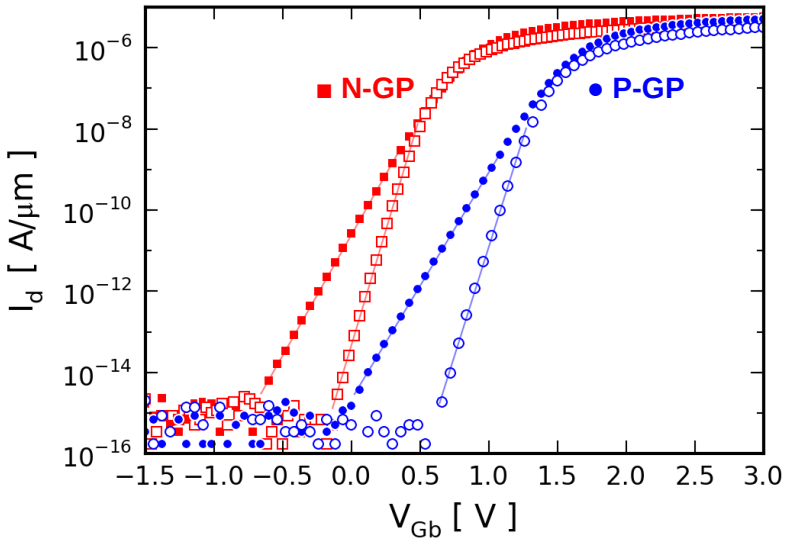

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- **NPN Characterization**
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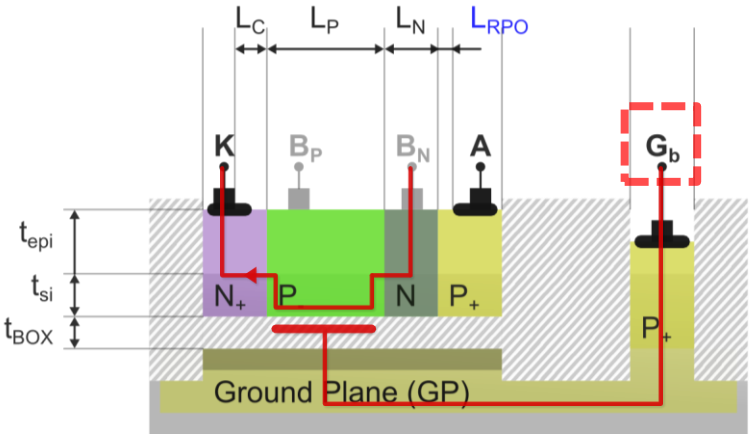
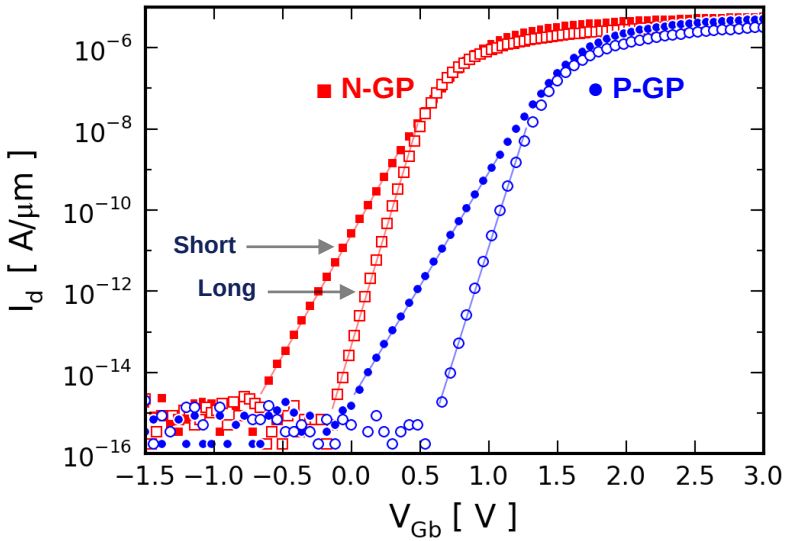
  - **Short channel swing is degraded :**
    - L_P = 500nm : S ≈ 95mV/dec
    - L_P = 200nm : S ≈ 175mV/dec





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    - L_P = 500nm : S ≈ 95mV/dec
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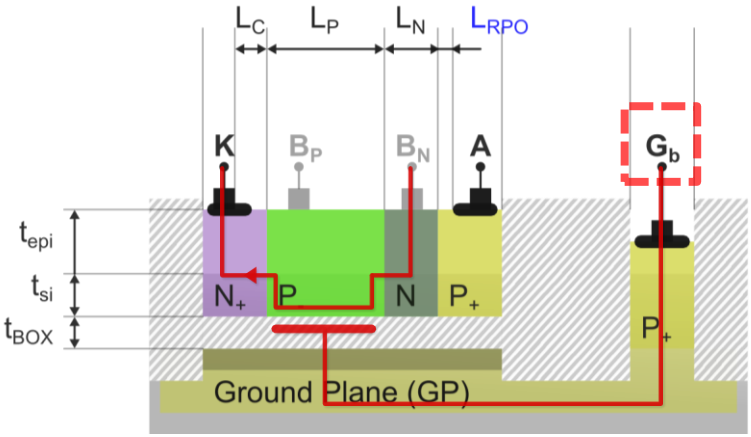
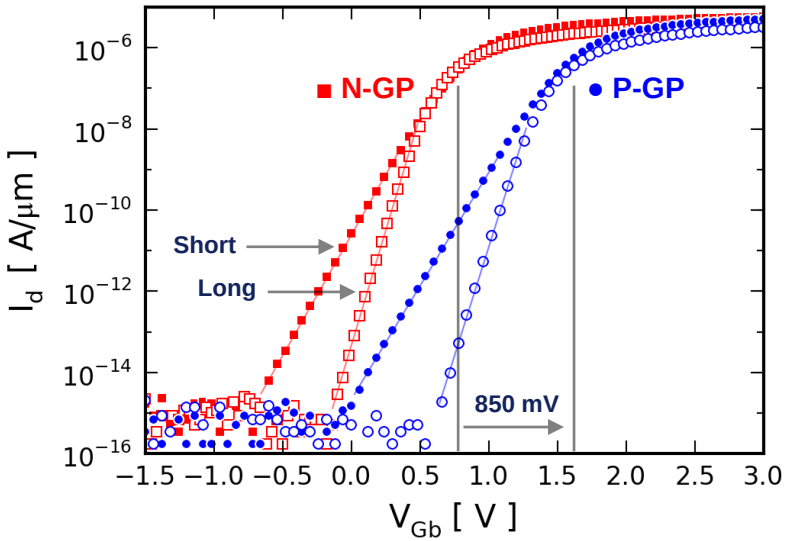
  - **V_{th} shift: +850mV**
    due to GP-type (workfunction difference between N and P-GP)





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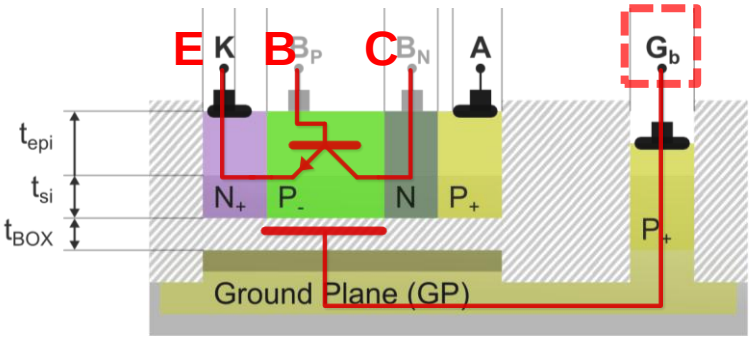
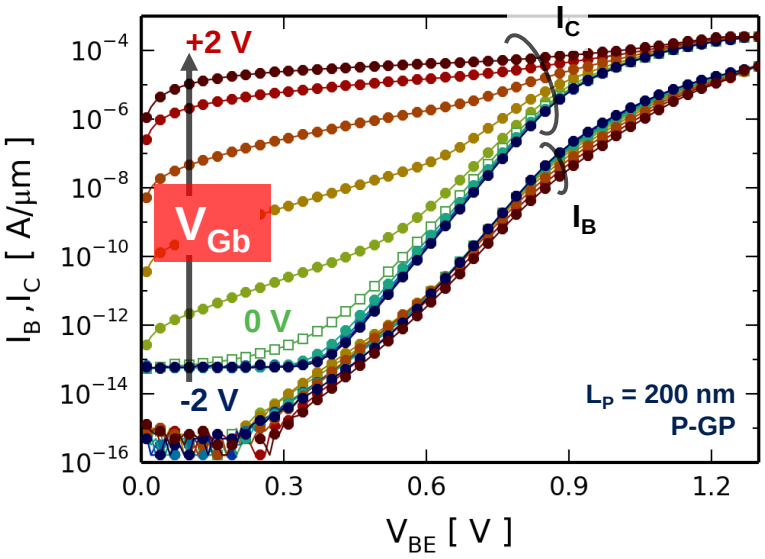
- **The NPN bipolar is effectively Modulated !**
  - **The NPN base potential is modulated by V_{Gb}**
  - **The Base-Emitter barrier depends on V_{Gb}**
  - **V_{Gb} ↗ ⇒ $I_{C\,eff}$ ↗**





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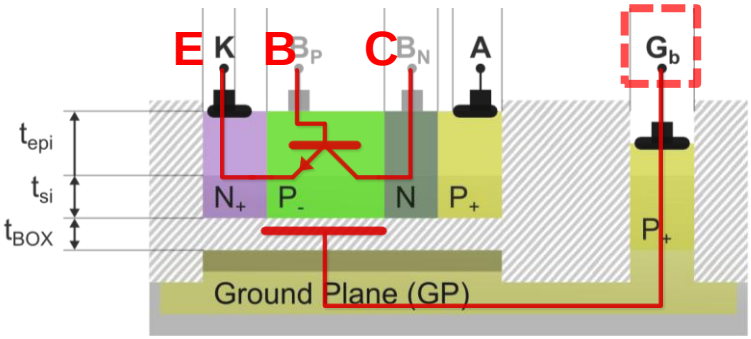
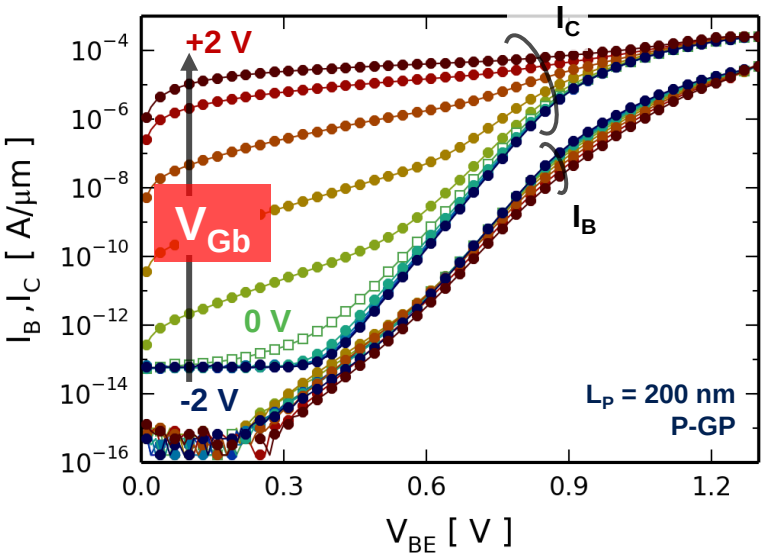
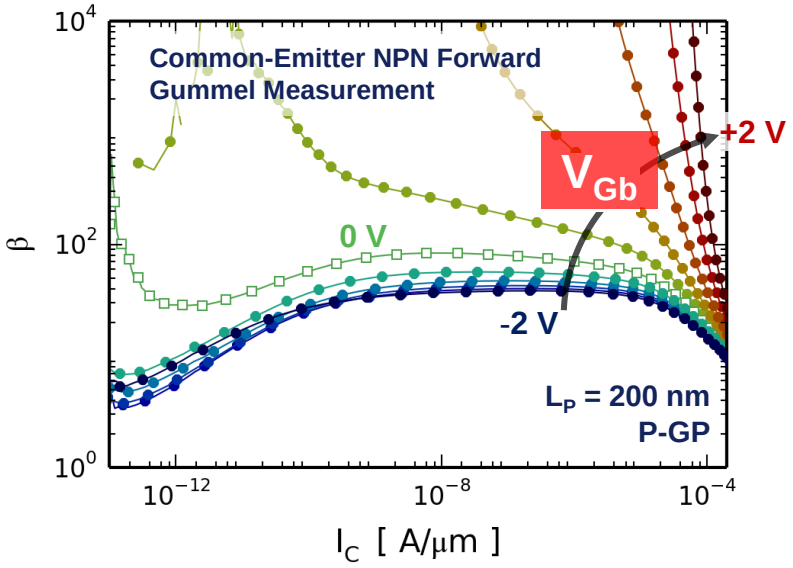
  - $V_{Gb} \nearrow \Rightarrow I_{C\,eff} \nearrow \Rightarrow \beta_{NPN\,eff} \nearrow$ [1]

[1] Colinge, IEEE TED, 1987.







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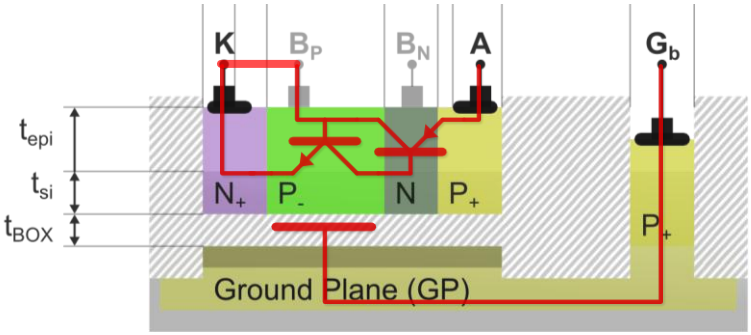
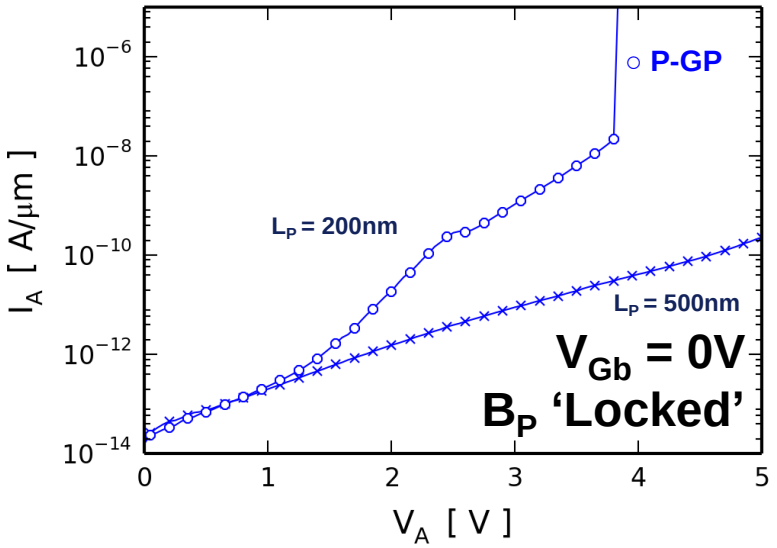
- **NPN Modulation changes SCR triggering**



- V_{Gb} ↗ ⇒ $I_{C\ eff}$ ↗ ⇒ $\beta_{NPN\ eff}$ ↗ ⇒ I_{t1}, V_{t1} ↘
- **SCR Triggering point (I_{t1}, V_{t1}) is set by β_{NPN} (L_P …)**



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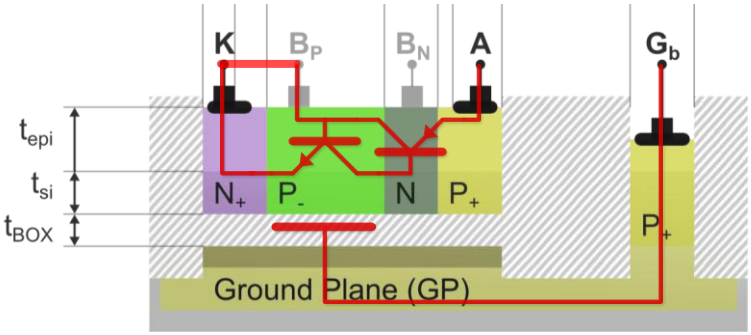

- V_{Gb} ↗ ⇒ $I_{C\ eff}$ ↗ ⇒ $\beta_{NPN\ eff}$ ↗ ⇒ I_{t1}, V_{t1} ↘
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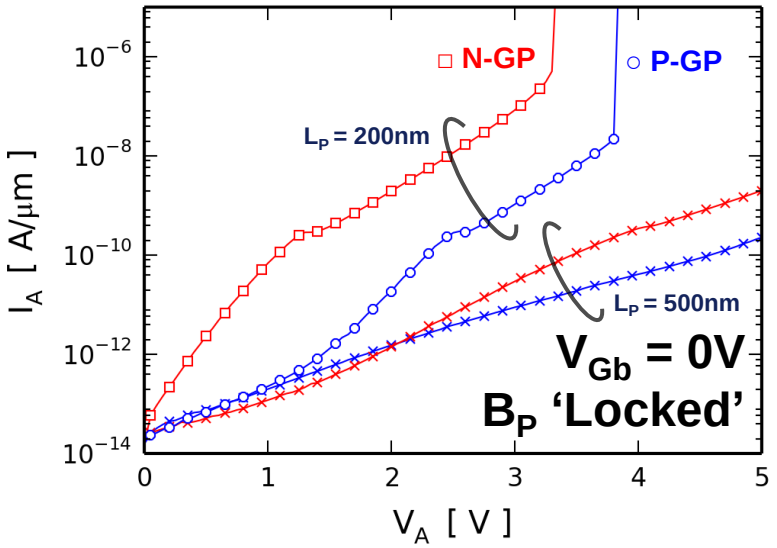

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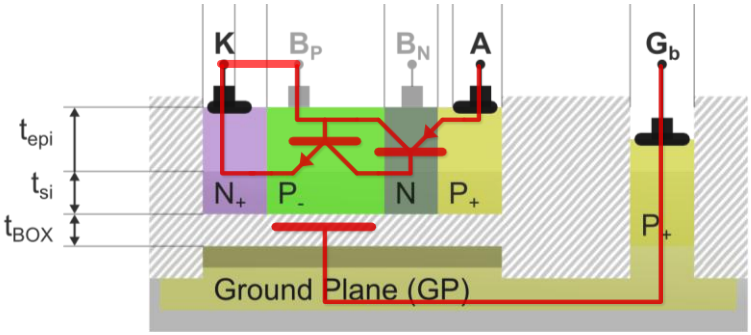

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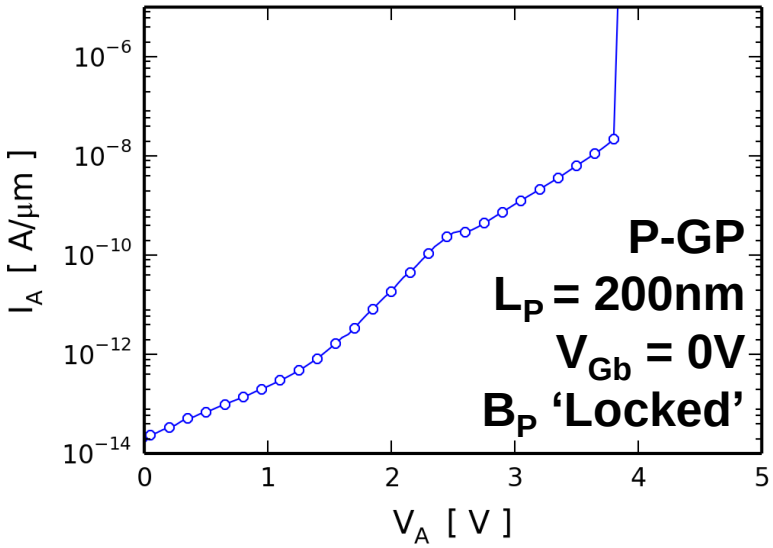

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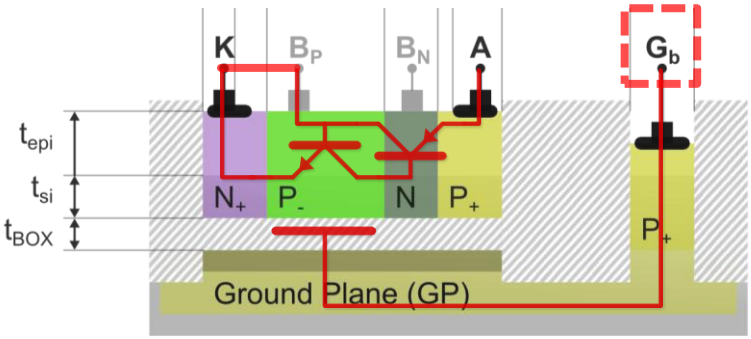

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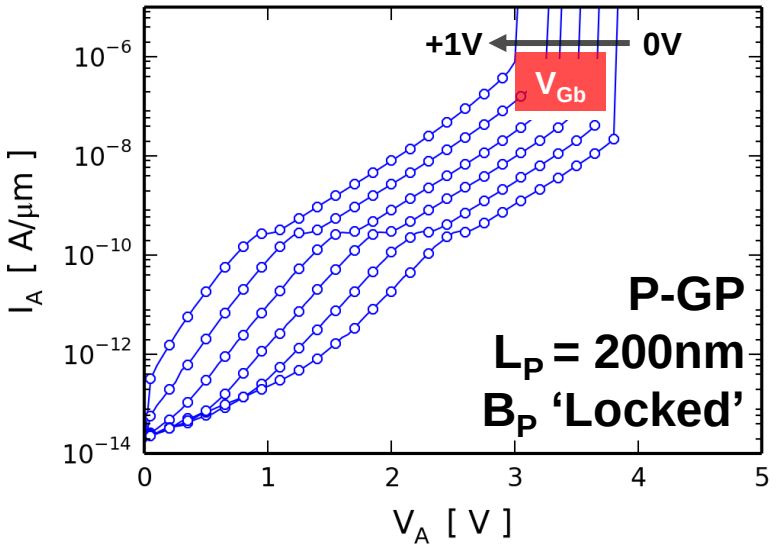

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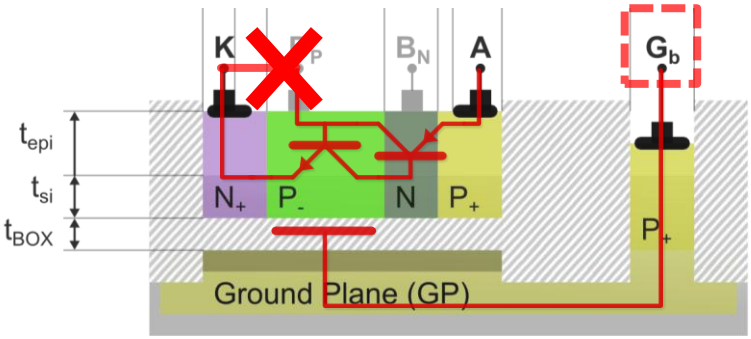

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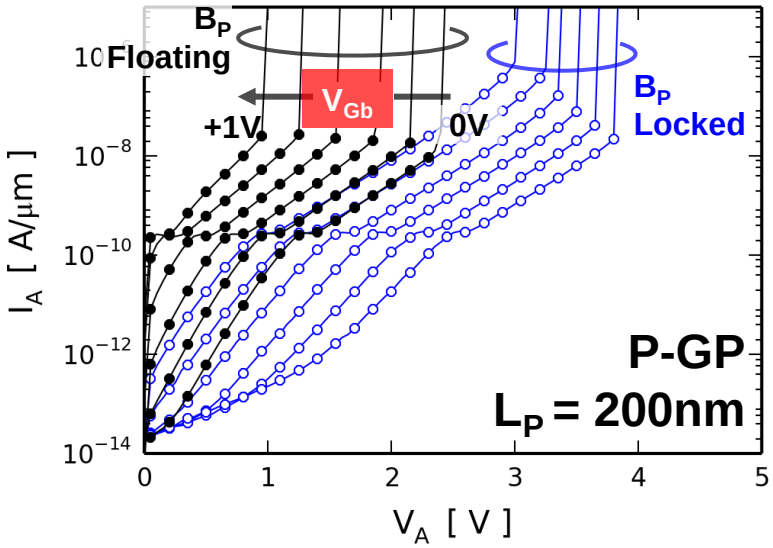
- **Strong capacitive coupling between P-base and back-gate allows floating-mode operation**



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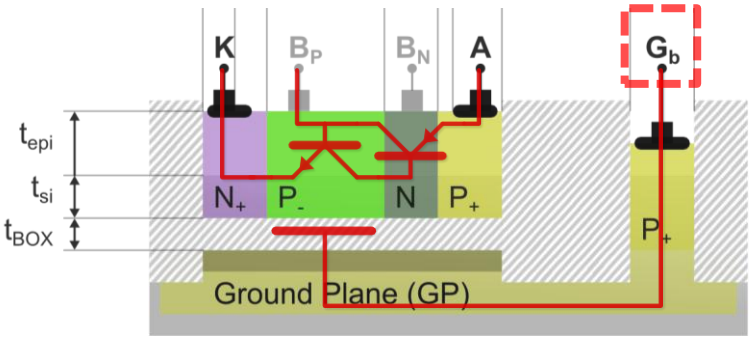

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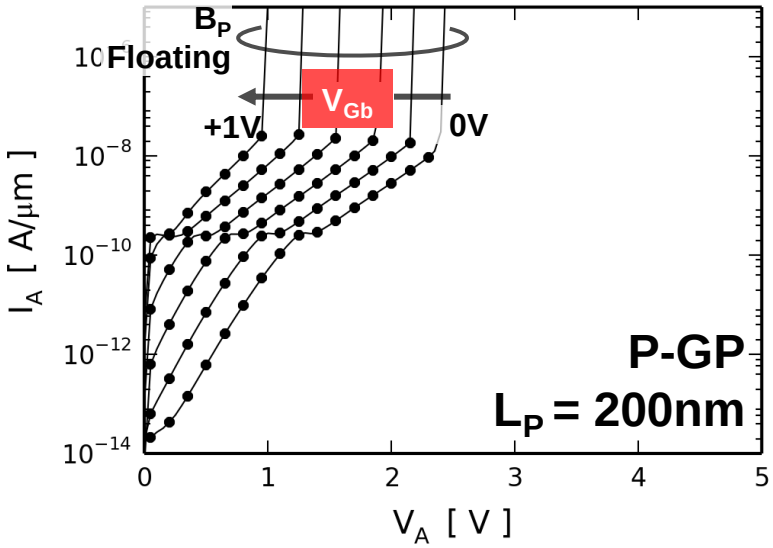

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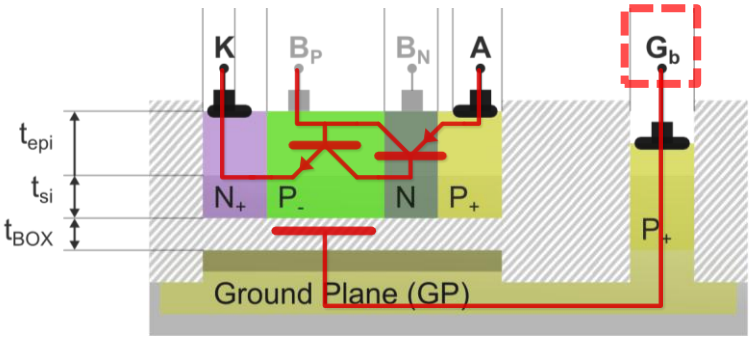

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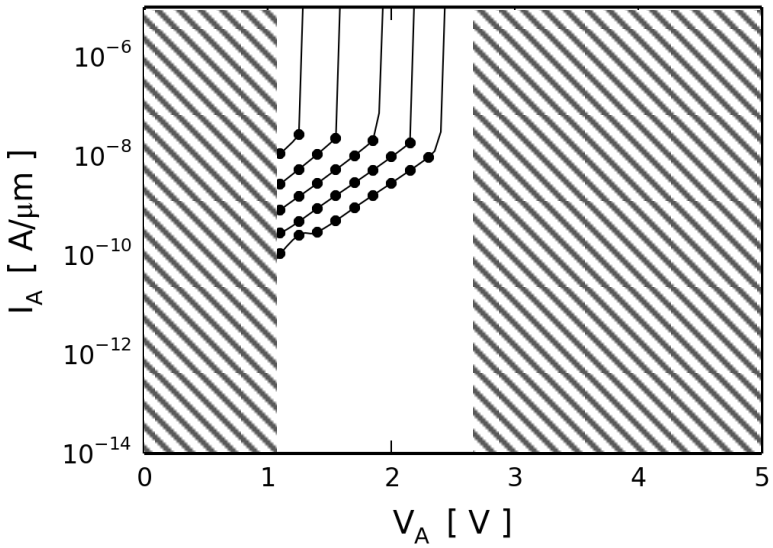

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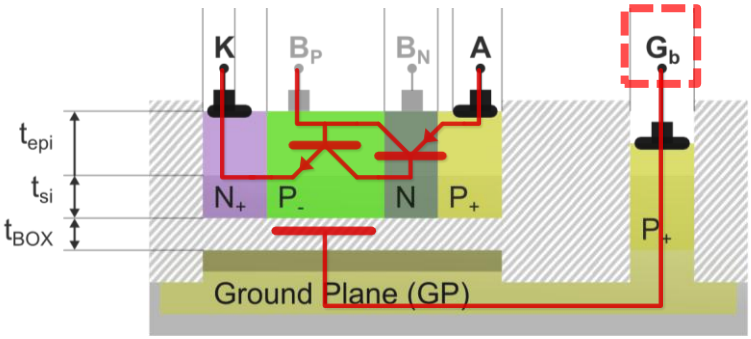

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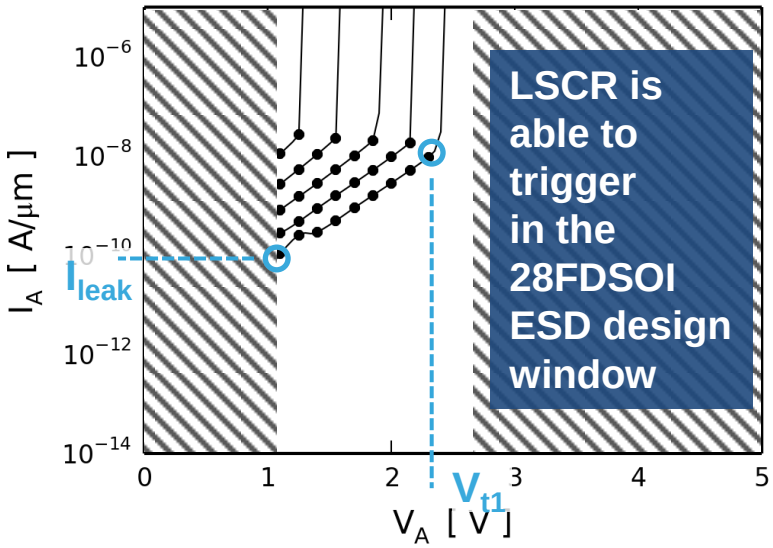

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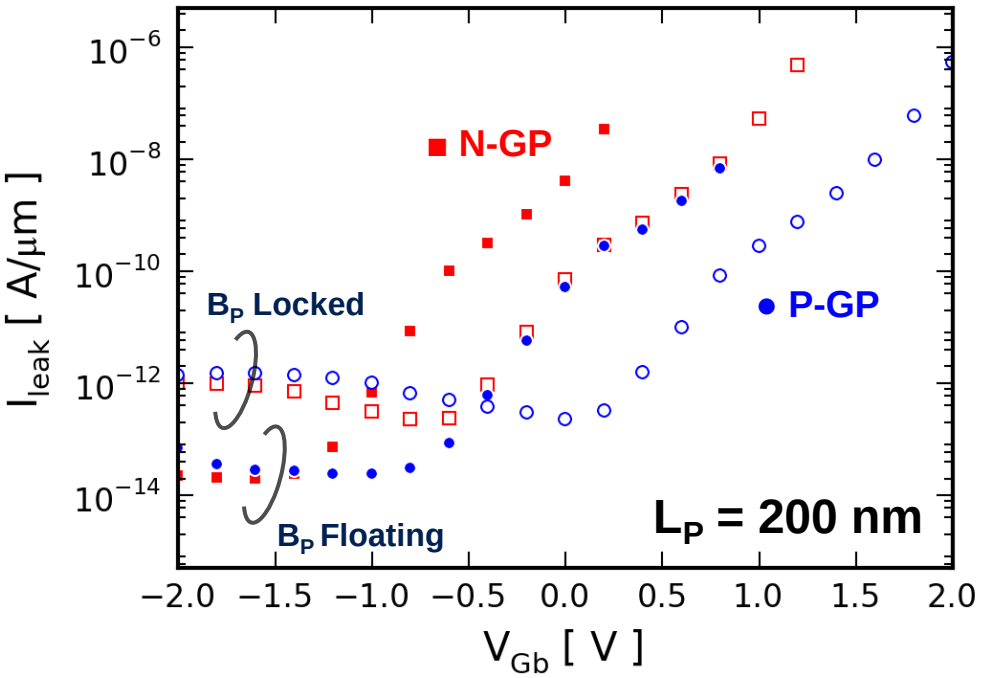
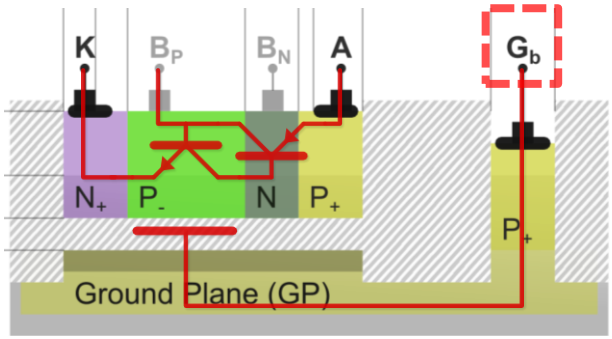
Experimental Results

- **SCR Leakage @ V_{dd} = 1V**
  - **Stronger Base-Emitter barrier means lower leakage**





	N-GP		P-GP	
	'Floating'	'B_p locked'	'Floating'	'B_p locked'
I_{leak} @ V_{Gb} = 0V	7 nA/µm	100 pA/µm	93 pA/µm	**0.5 pA/µm**
I_{leak} @ V_{Gb} = -1V	0.9 pA/µm	0.7 pA/µm	**17 fA/µm**	1.1 pA/µm

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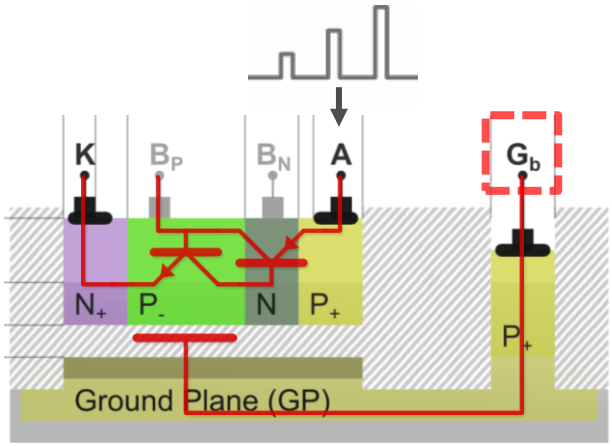
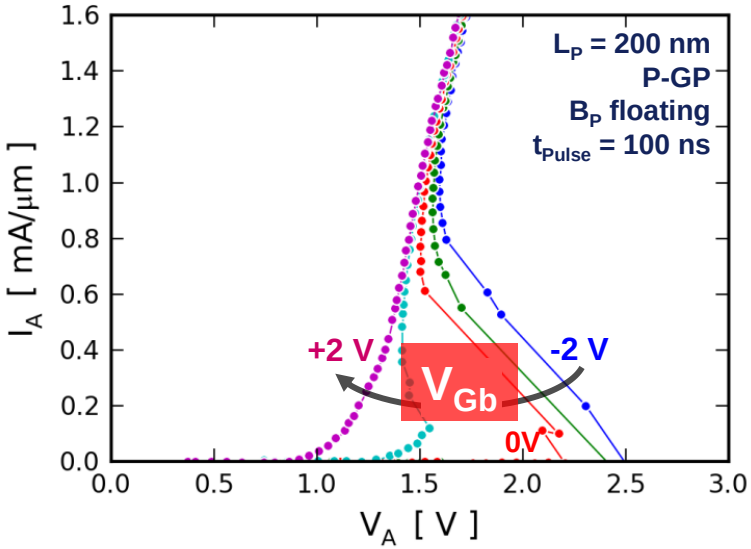
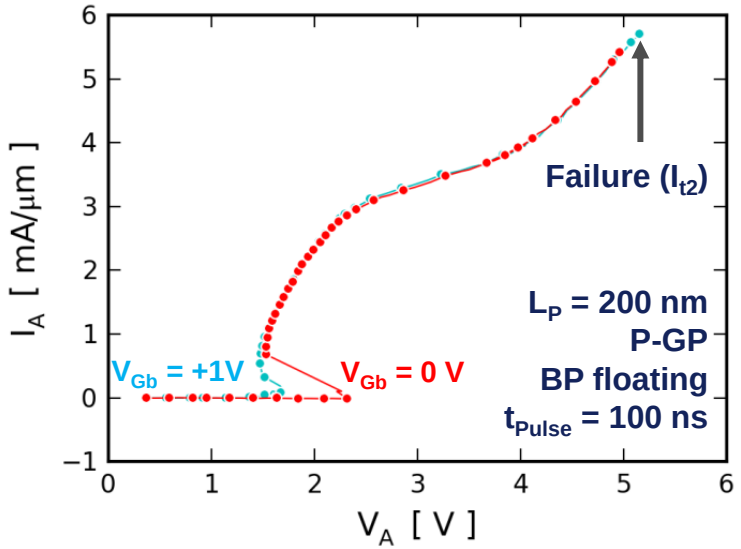
Experimental Results

- **Transmission Line Pulse (TLP) High-Current measurements**
  - **No need of Base contacts**
  - **V_{t1} adjustment with V_{Gb} is confirmed**
  - **Performance: $I_{t2} \approx 5mA/\mu m$ (TLP 100 ns)**







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Conclusions

Conclusions

- LSCR **experimentally demonstrated** and understood via TCAD in an Ultra-Thin-SOI technology:
  - I_{leak} < 20 fA/µm is achievable with adequate V_{Gb}
  - « Tunable V_{t1} » (adjustable to application) with Back Bias, GP-type, NPN Base length
- **Controlled only with back gate biasing** : No need of Base Contacts or Front Gate
- SOI-LSCR is fully compatible with standard FDSOI CMOS process
- TLP performances (ESD failure current) validates I_{t2}≈5mA/µm
- Adequate for « Core MOS » protection in 28nm FDSOI


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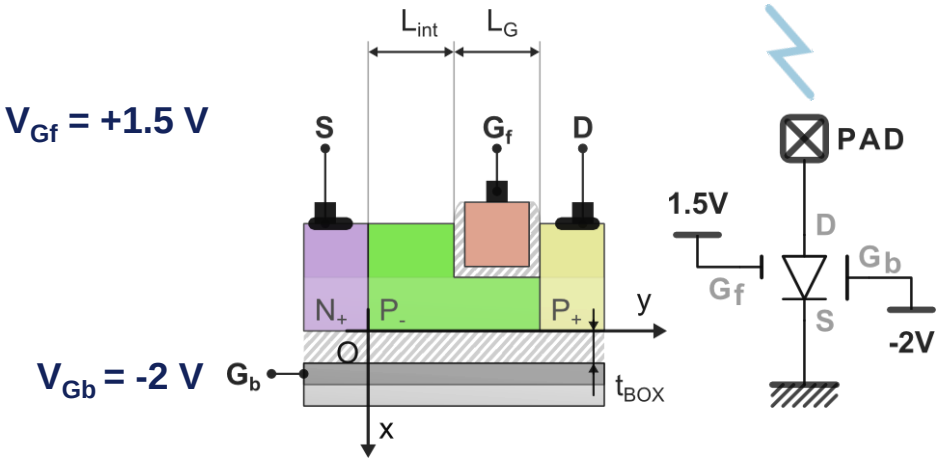
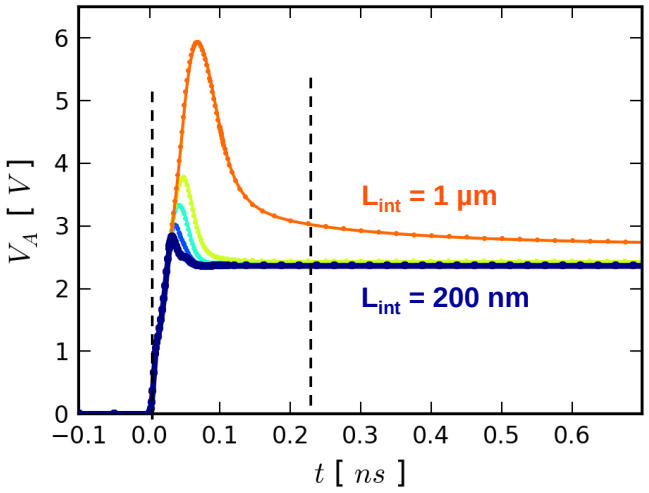
BackUp Slides

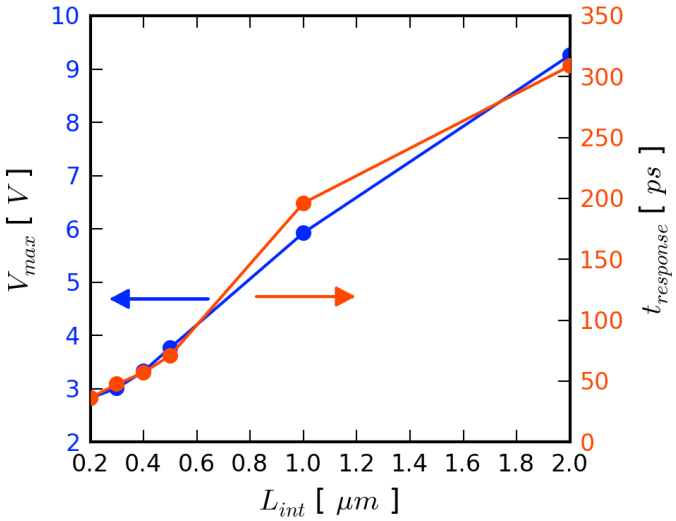
Transient Characteristics for ESD

- **Transient & ESD Applications**





- **Voltage Pulse with 50 ps RT and I_A = 1mA/µm**
- **For decreased L_{int} :**
  - **Overshoot Peak Voltage decreases from 9V to 3V**
  - **Device response time ↘ (< 50 ps)**



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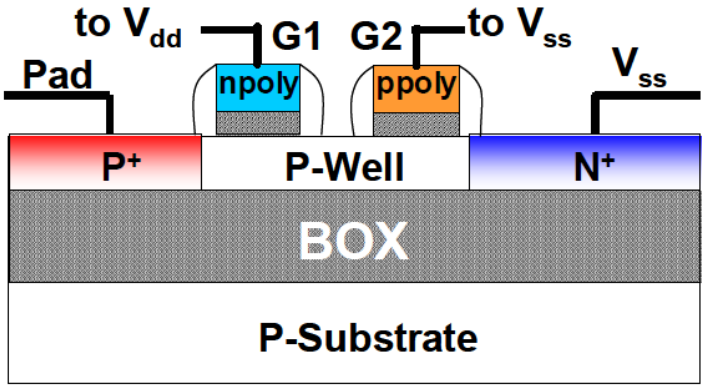
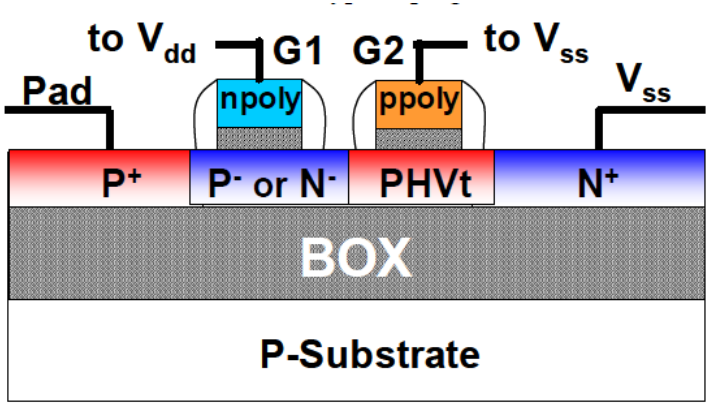
- [Salman et al. 2006] [Cao et al. 2011]



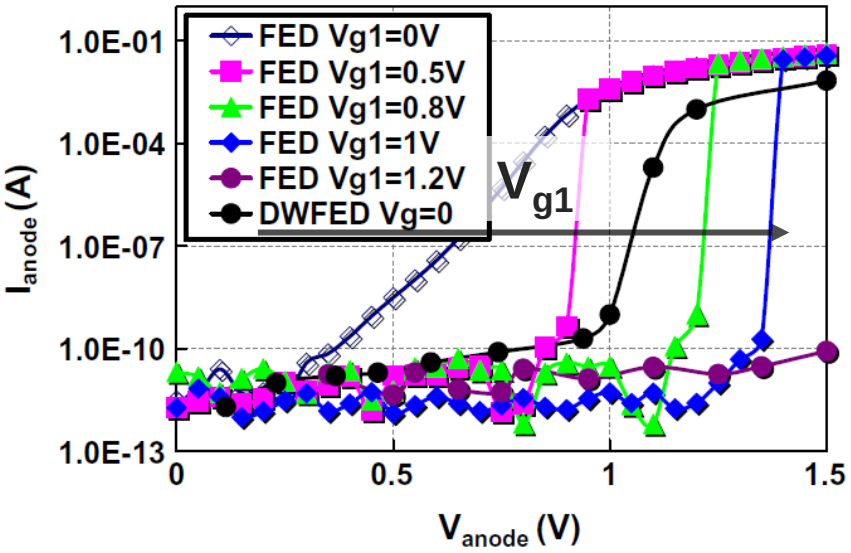


V_{g1} controls the inversion in the (P-) region and change the triggering voltage of the structure

t_{Si} = 70nm t_{BOX} = ?

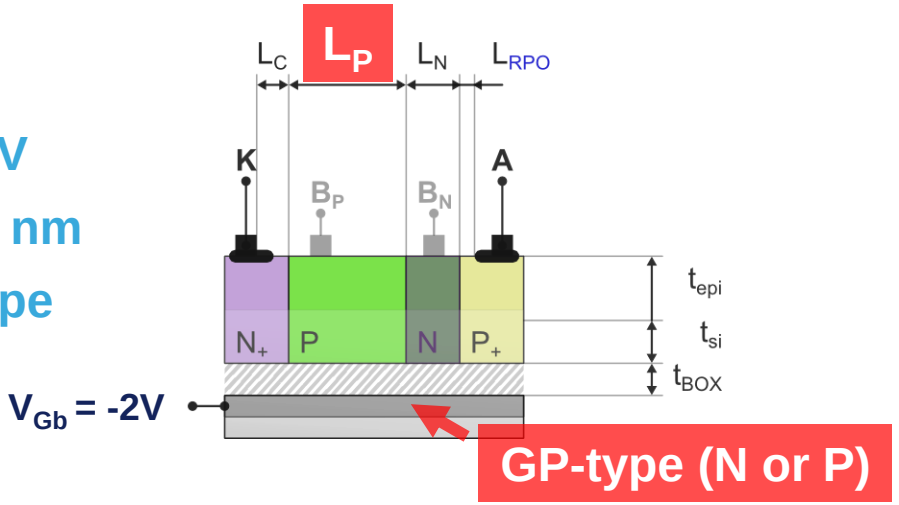
doped: "P+/P-/HVt/N+ FED"

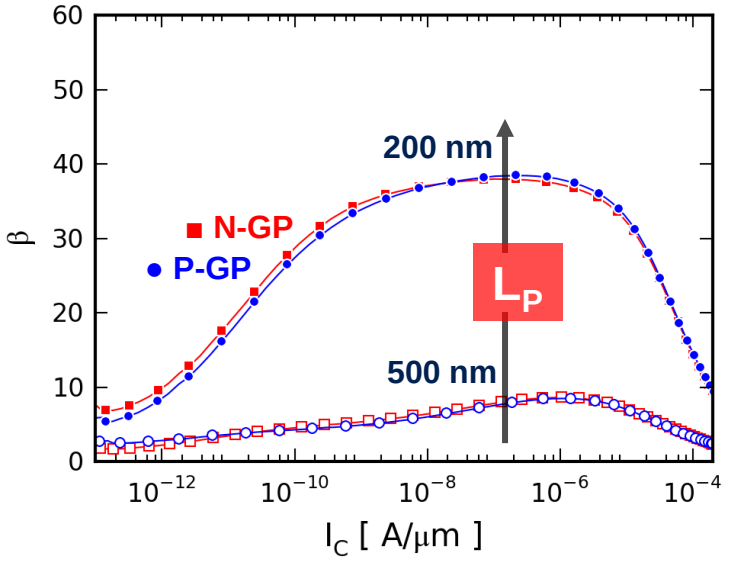
$L_{g1} = L_{g2} = 0.5$ µm, L_{gap}?

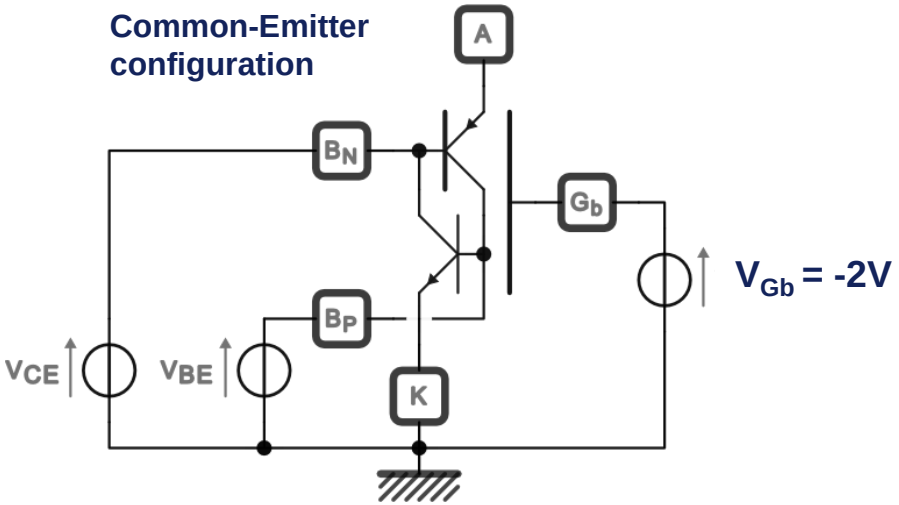


LSCR Characterization

- **NPN Gain in accumulation**
  - Accumulation condition V_{Gb} = -2V
  - **2 designed Bases:** L_P=200 & 500 nm
  - No dependance of β_{NPN} on GP type
  - $\beta_{NPN} \approx 40$ with L_P=200 nm







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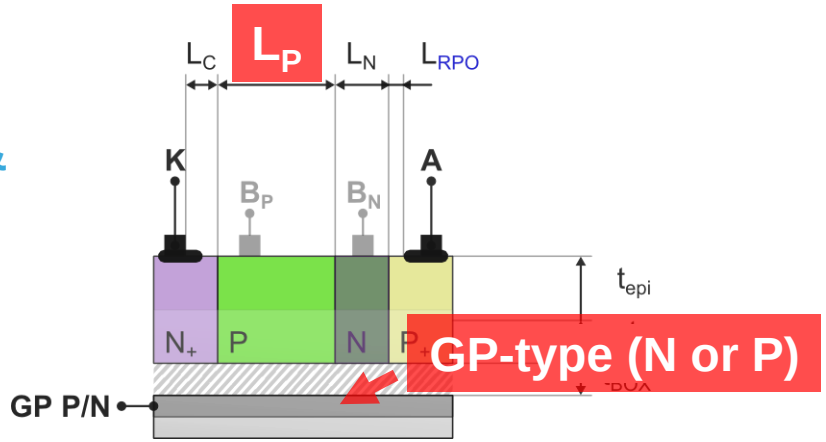
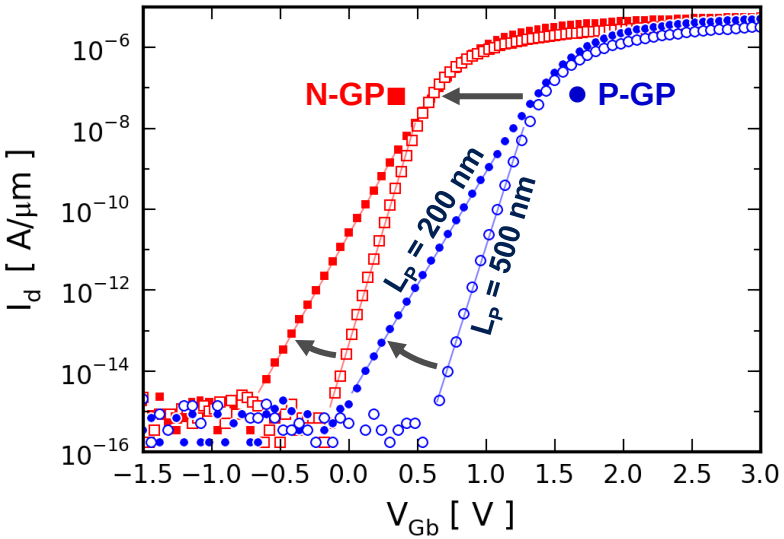
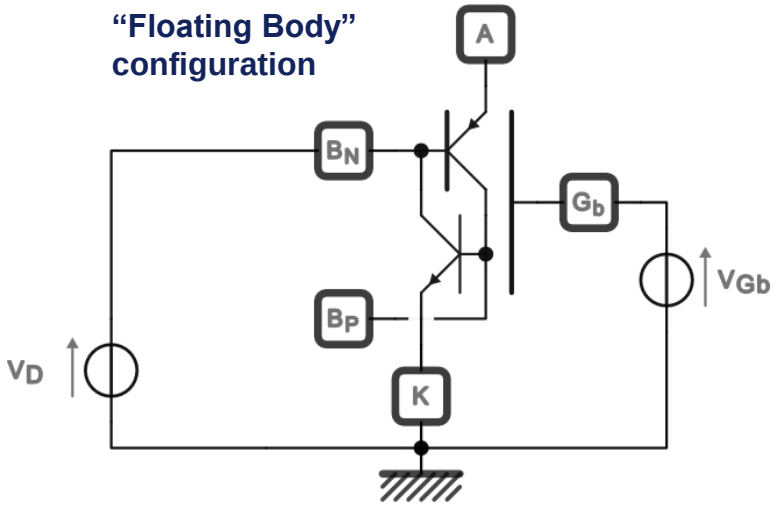
LSCR Characterization

- **NPN = « Back-Channel » NMOS**
  - **NMOS Extraction of Threshold [1] & Swing in linear regime (V_D = 20mV)**
  - **850mV V_{th} shift N-GP to P-GP**
  - **S = 95 mV/dec to 175 mV/dec**



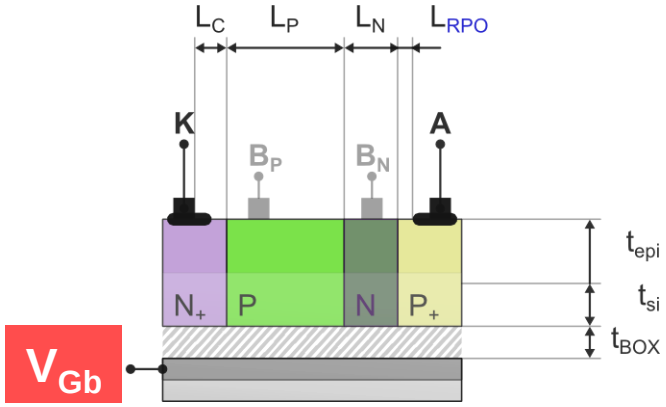


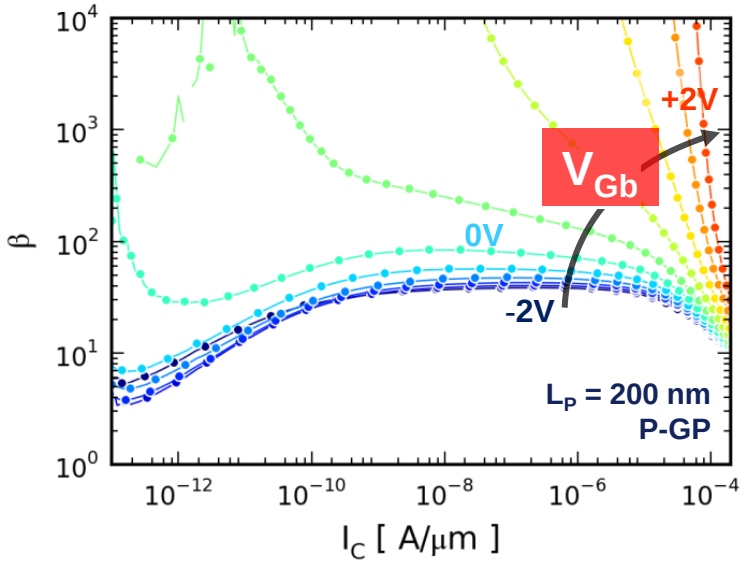


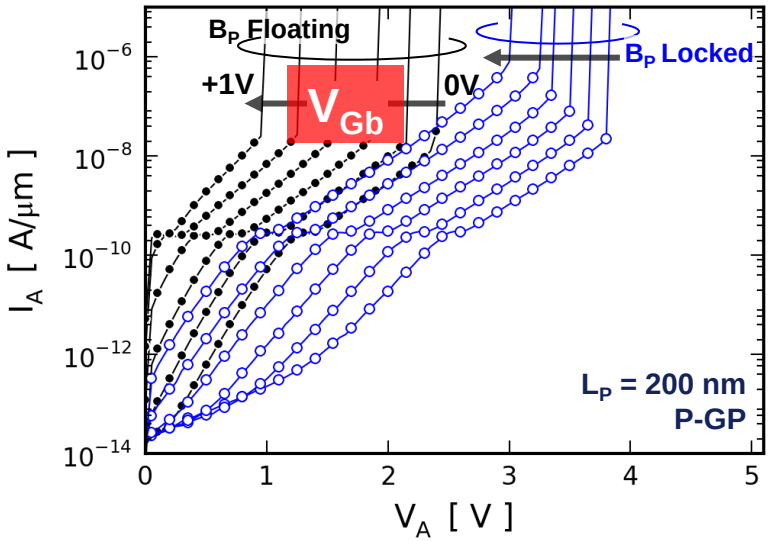
[1] Ghibaudo et al. Electronics Letters, 1988

LSCR Characterization

- **Effective NPN Gain control**
  - $\beta_{NPN\ eff}$ is dramatically increased by back NMOS I_D current
  - V_{Gb} < -1V allows a strong diminution of I_{leak} (20fA/µm)
  - $\beta_{NPN\ eff}$ ↗ : I_{t1}↘ & V_{t1}↘







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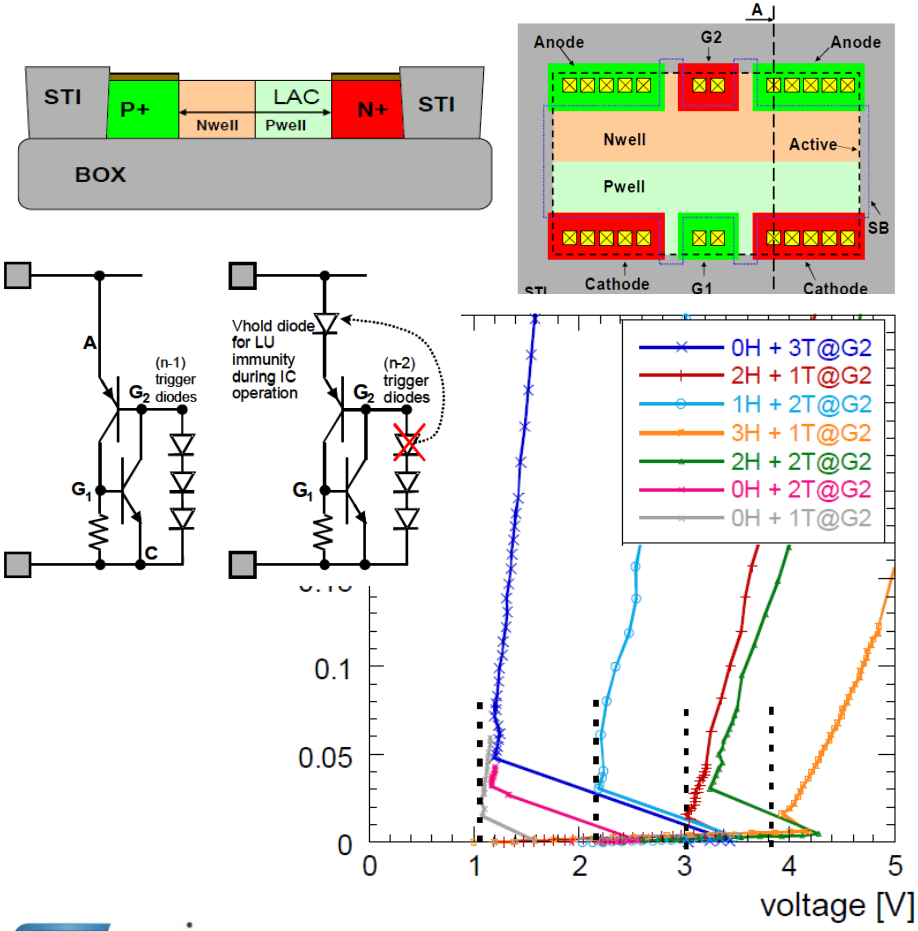
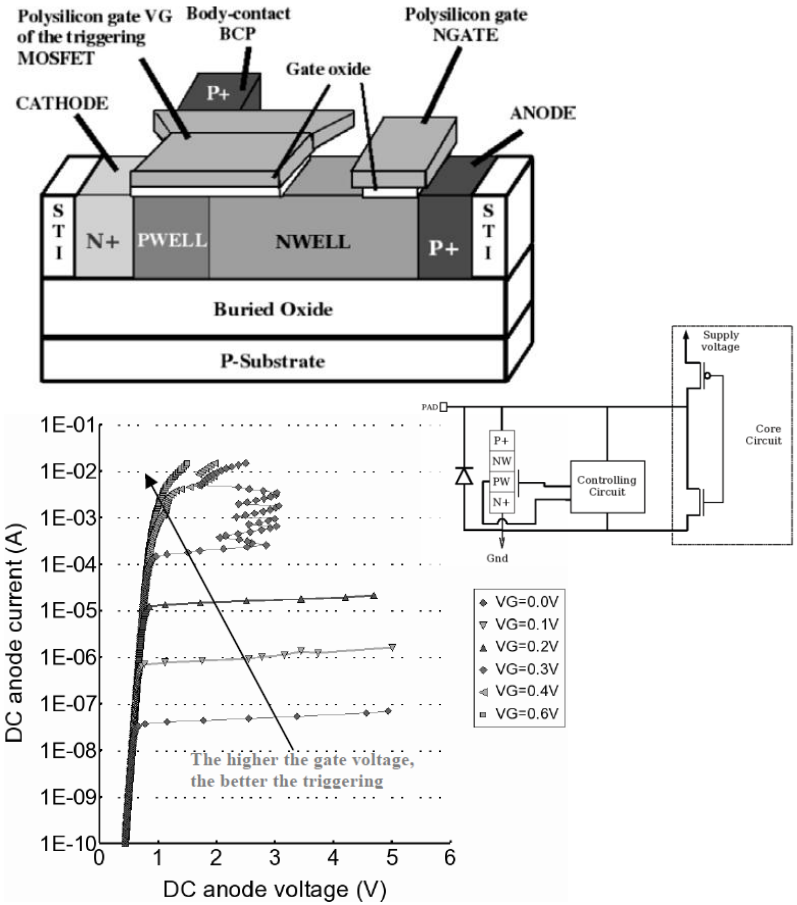
LSCRs

- **State of the Art**

[Marichal et al. EOS/ESD 2005]



[Entringer et al. EOS/ESD 2006]



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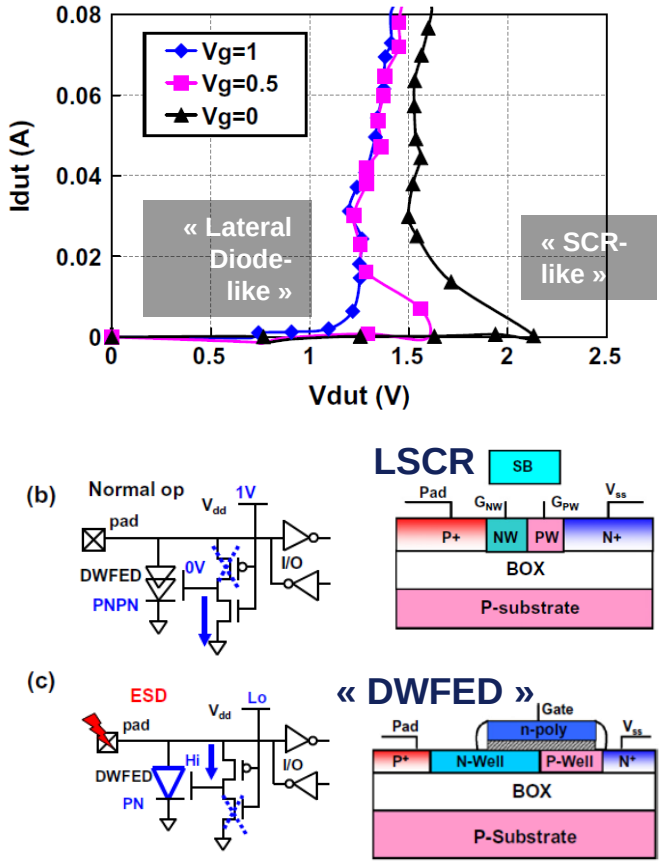
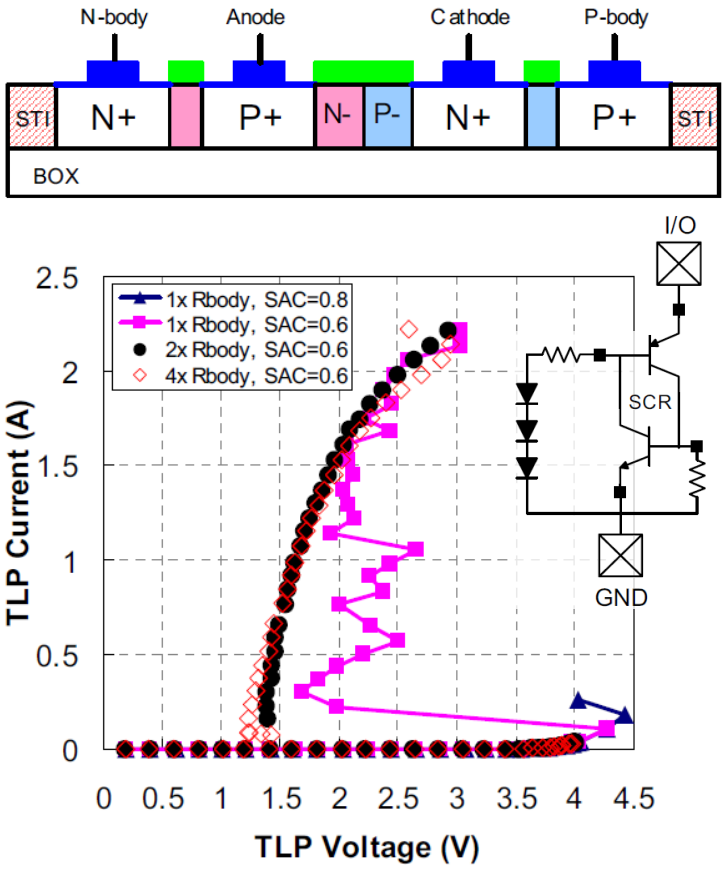
[Cao et al. Microelectronics Reliab, 2011]



[Li et al. EOS/ESD, 2012]



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