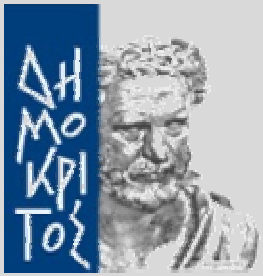

Porous Si Dielectric Parameter Extraction for use in RF Passive Device Integration: Measurements and Simulations

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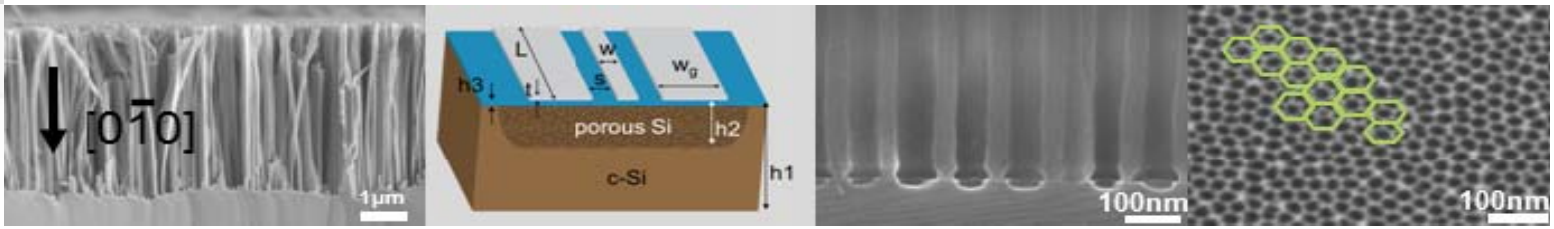


Outline

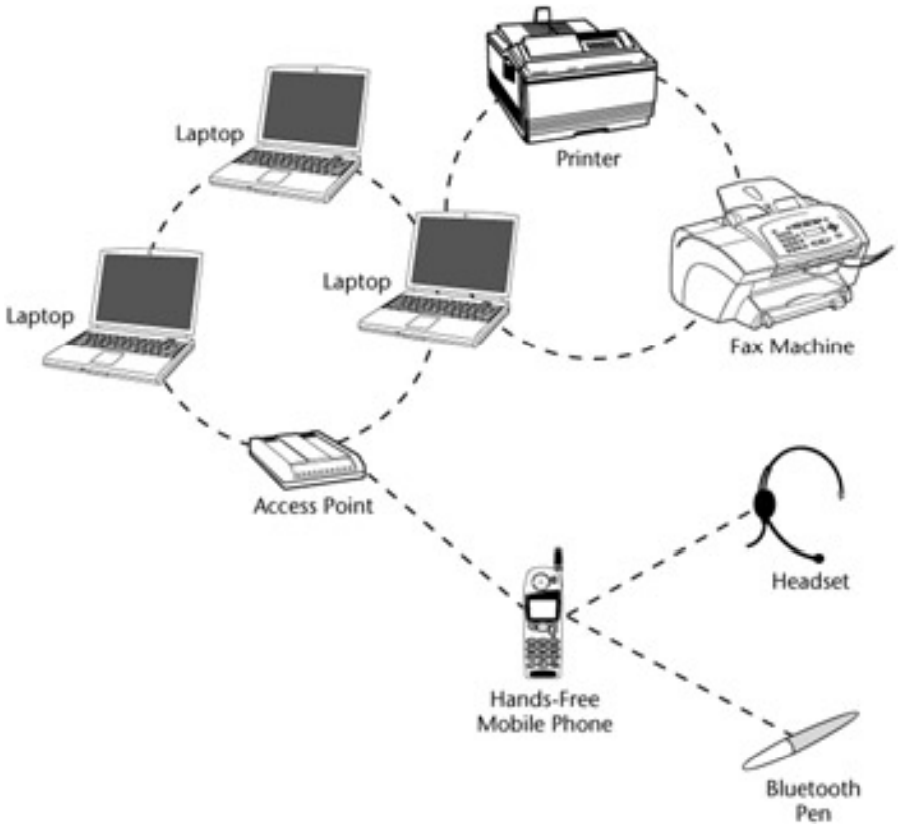
1. Introduction
2. Porous Si as an RF material
3. Dielectric Parameters of porous Si
4. Dielectric Characterization of porous Si
   - 4.1. Evaluation of the Characterization Method
   - 4.2. Comparison between Measurements and Simulations
5. High-performance RF devices on porous Si
6. Conclusions

Introduction

- Why RF circuits?
  - Wireless Communications

Higher Frequencies ↓ Shorter Wavelengths

FM (100 MHz):	3 m
GSM (900 MHz):	33 cm
Wi-Fi (2.4 GHz):	12.5 cm
Q-band (33-50 GHz):	9-6 mm
W-band (75-110 GHz):	4-2.7 mm



- Why on-chip RF circuits?
  - Cost reduction.
  - Reduction of losses and parasitics due to wirebonds.

On-chip RF circuits - Bottlenecks

Standard CMOS silicon (1-10 Ω.cm) is

- a very lossy material => **high RF losses in the substrate**
- a high ε_r material (11.7) => e.g. **high crosstalk**

This mainly affects:

- Integration of RF passive devices *(Tlines, inductors, filters …)*
- Integration of antennas

Some examples ….

1. Difficult to achieve high Zc transmission lines
2. Difficult to achieve inductors that resonate at high frequencies
3. High energy loss in the surface waves inside the substrate

On-chip RF passives – Solutions for high performance

- On chip solutions under investigation
  - New topologies:

    > patterned metal shield below the devices e.g. Slow-wave CPW

    moderate-losses, CMOS processing, low-cost

    ...not applicable to all devices

  - Trap-rich HR-SOI

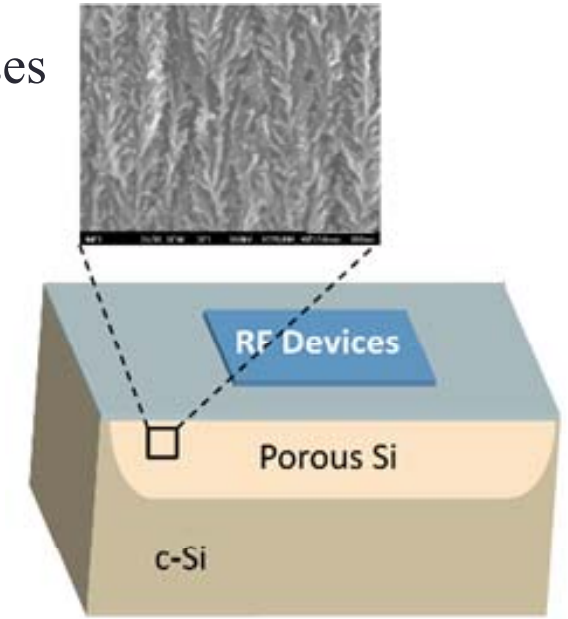
    > HR-Si with a trap-rich layer for use in SOI processes

    low-losses, SOI CMOS processing, expensive

  - **Porous Silicon**

    > local formation of porous Si on a bulk wafer, underneath the passive devices

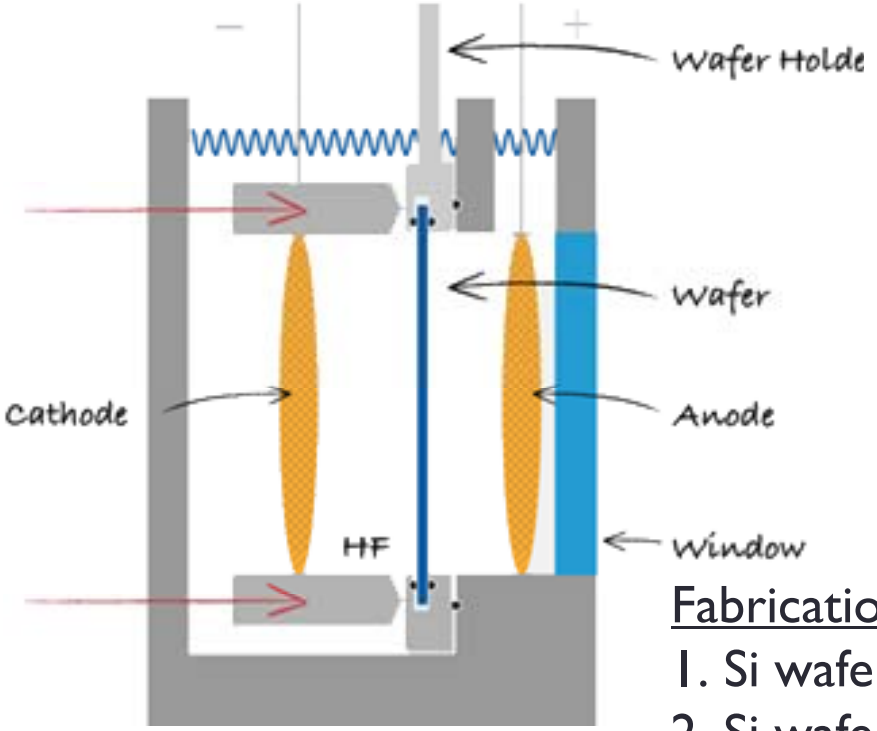
    low-losses, compatible with batch Si processing, low-cost



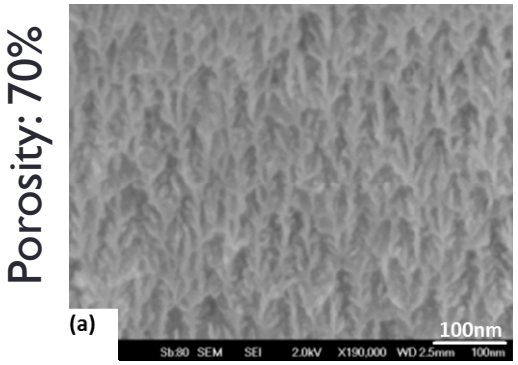
What is Porous Silicon ?

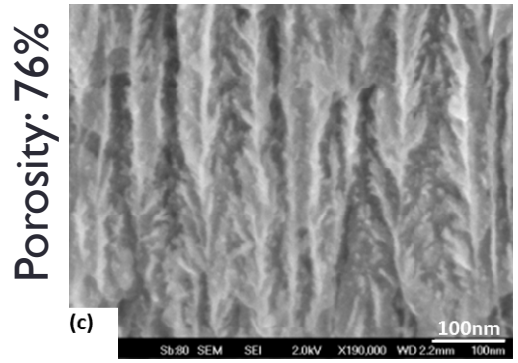
- Formation:

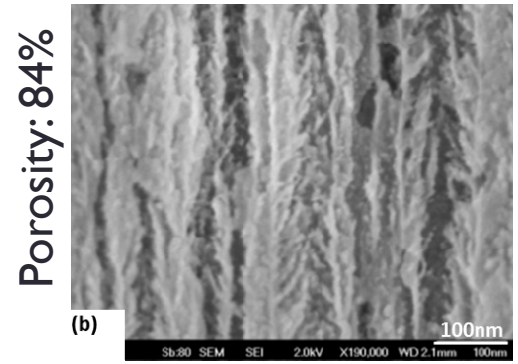
  > *Electrochemical dissolution of Si in HF solution*



courtesy of AMMT GmbH







Fabrication Parameters:

1. Si wafer Type
2. Si wafer Resistivity
3. Electrolytic Solution
4. Anodization Current

Porous Silicon as an RF material

- Dielectric parameters of porous Si are highly dependent on

Porosity, Structure, Morphology

↓

Tunability of ε_r and tanδ

==> Need for accurate and reliable parameter extraction for the specific material used

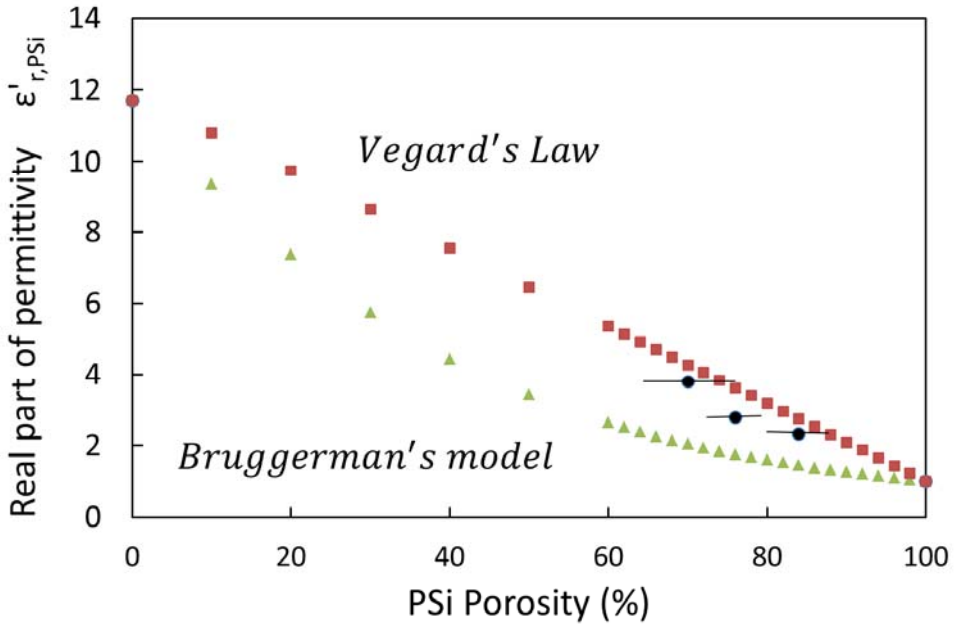
TARGET: To have a **reproducible** material with the **desired** and **well characterized** parameters which can be used in **RF simulation** tools resulting in good agreement between simulation and measurements

Dielectric Parameters of Porous Si

- Tunable ε_r
  - range: 2-9
    (c-Si: 11.7 @ 25 °C)
- Low loss tangent
  - ~0.02-0.05
- Stable dielectric parameters over T
  - T=20-170°C

Increased porosity > reduced dielectric constant

The experimental values of ε_r are in-between the values predicted by Vegard's and Bruggerman's models.



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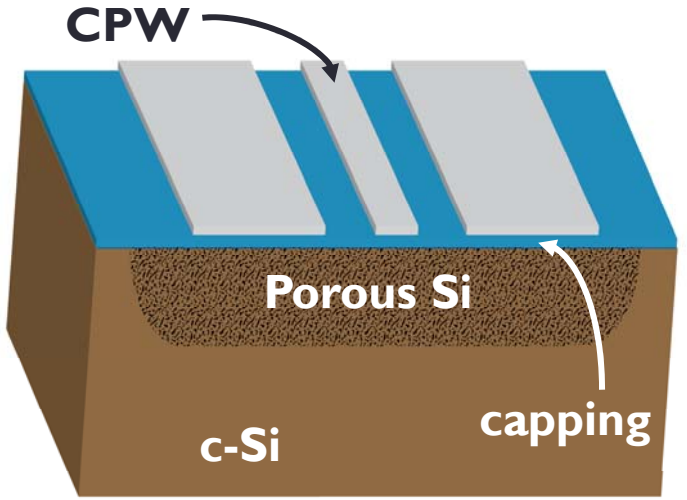
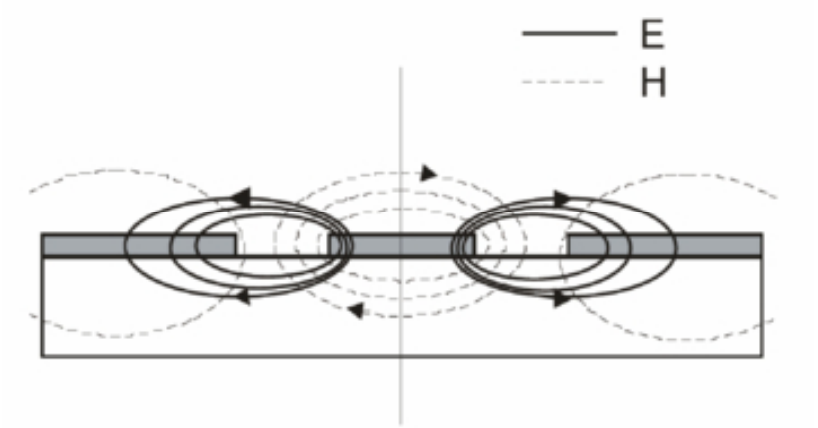
Porous Silicon Characterization Method

- Dielectric Characterization
  1. Fabrication of the PSi layer
     (p^+, porosity 75%, 200 μm thick)
  2. Integration of a Coplanar Waveguide (CPW) on it
  3. S-parameters measurements
     (1-40 GHz)
  4. Conformal Mapping Method
     - Quasi-TEM mode
     - Valid until 400 GHz





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Parameter Extraction

- Extraction of $\varepsilon_{r,PSi}$

$$\varepsilon_{eff} = 1 + q_1(\varepsilon_{r,Si} - 1)$$

(eq. 1)

$$+q_2(\varepsilon_{r,PSi} - \varepsilon_{r,Si}) + q_2(\varepsilon_{r,cap} - \varepsilon_{r,PSi})$$

where $q_j = \frac{1}{2}\frac{K(k_j)}{K(k_j')}\frac{K(k_0')}{K(k_0)}, \quad j = 1,2,3.$

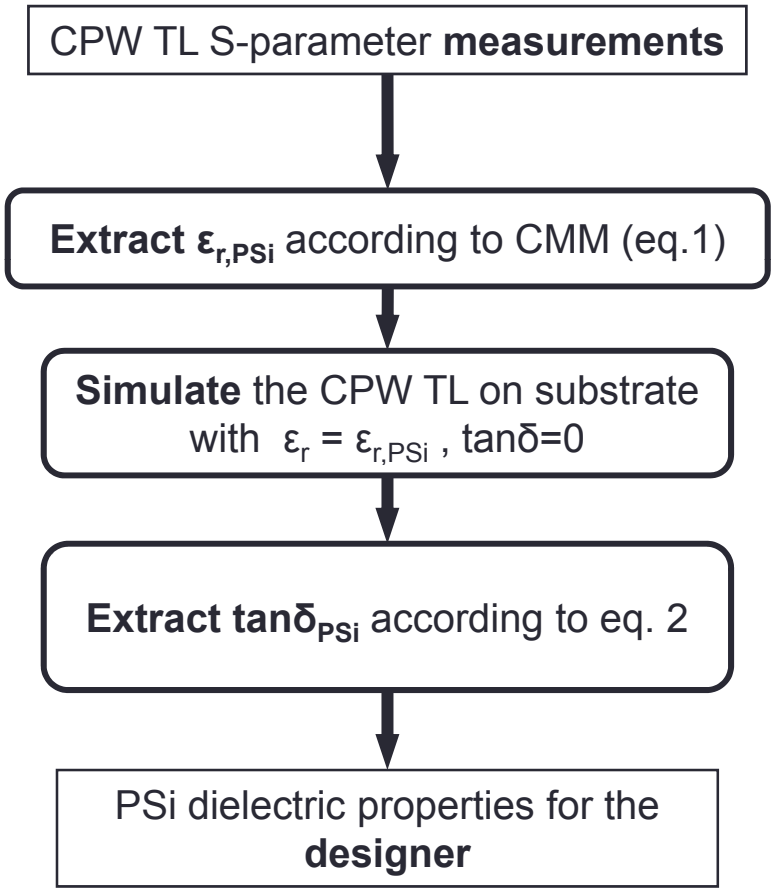
- Extraction of $tan\delta_{PSi}$

$$a_S = a_T^{PSi} - a_T^{Simulations}$$

(eq. 2)

$$= \frac{\pi f}{c \cdot \sqrt{\varepsilon_{eff}}} \cdot \begin{pmatrix} (q_1 - q_2)\,\varepsilon_{r,Si}' \cdot \tan\delta_{Si} \\ +(q_2 - q_3)\,\varepsilon_{r,PSi}' \cdot \tan\delta_{PSi} \\ +q_3\varepsilon_{r,cap}' \cdot \tan\delta_{cap} \end{pmatrix}$$

New Algorithm !



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Reliability of the Extraction Method

1. We have performed the extraction of the dielectric parameters on 6 different samples with 145 Ω CPW integrated on them
2. We have used the extracted values to simulate the same 6 devices using HFSS
3. We compare the simulations to the measurements

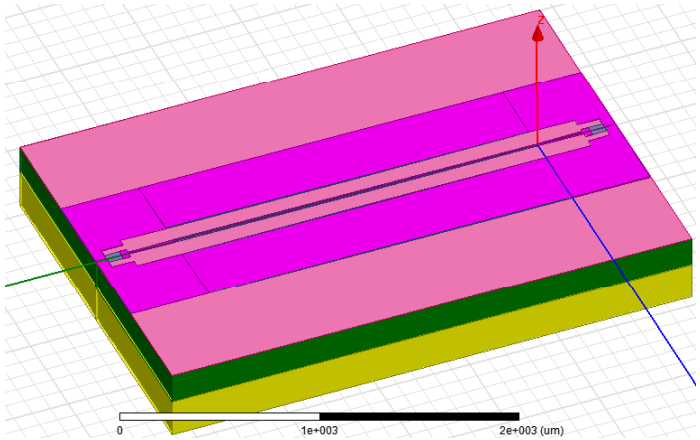
==>The maximum average deviation between measurement and simulation was:

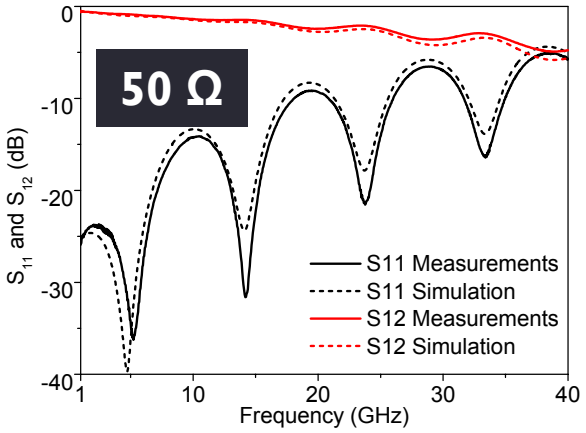
- 1.2 dB for S_{11}
- 0.5 dB for S_{12}

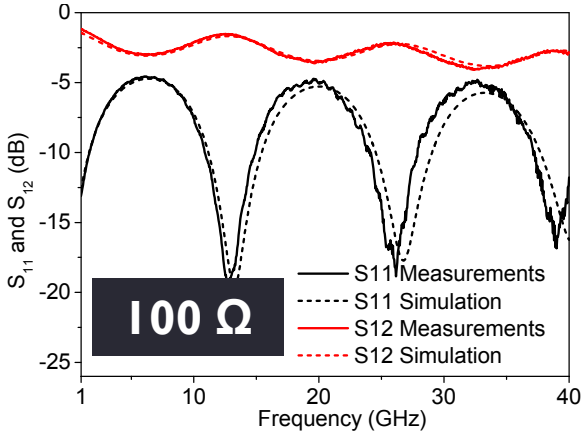
CPW Device	Zc [Ω]	E_{11} [dB]	E_{12} [dB]
CPW1	145	1.2	0.4
CPW2	145	1.1	0.5
CPW3	145	1.0	0.3
CPW4	145	0.6	0.3
CPW5	145	0.5	0.3
CPW6	145	0.5	0.2

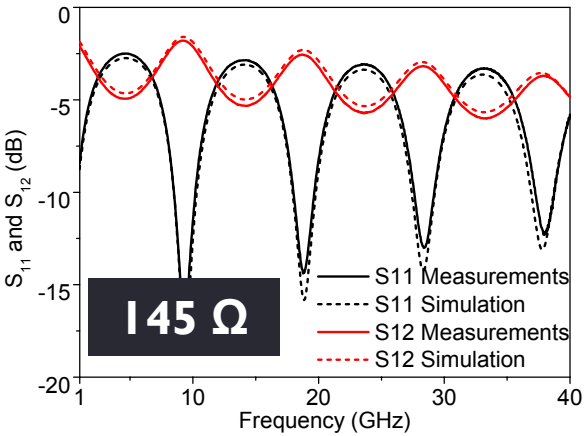
Measurement-Simulation Comparison I

- We extract the values of ε_r and tanδ of a PSi layer
- We feed these values into HFSS to simulate the performance of 50, 100, 145Ω CPW Tlines
- We compare the simulations to the measurements of devices fabricated on PSi



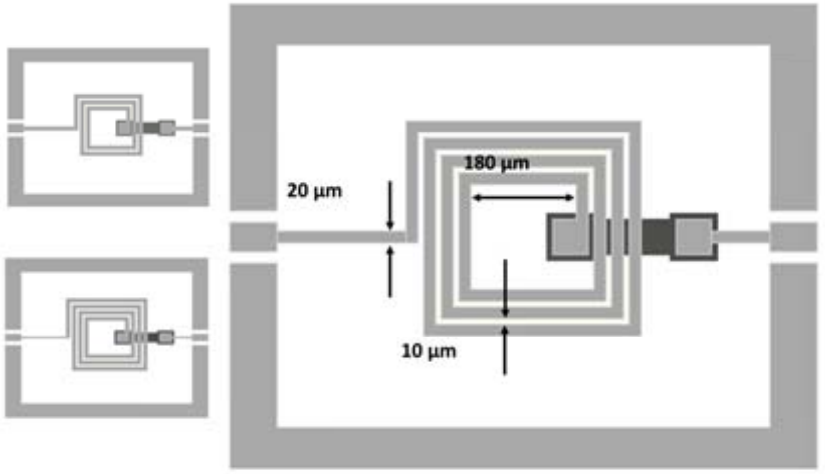


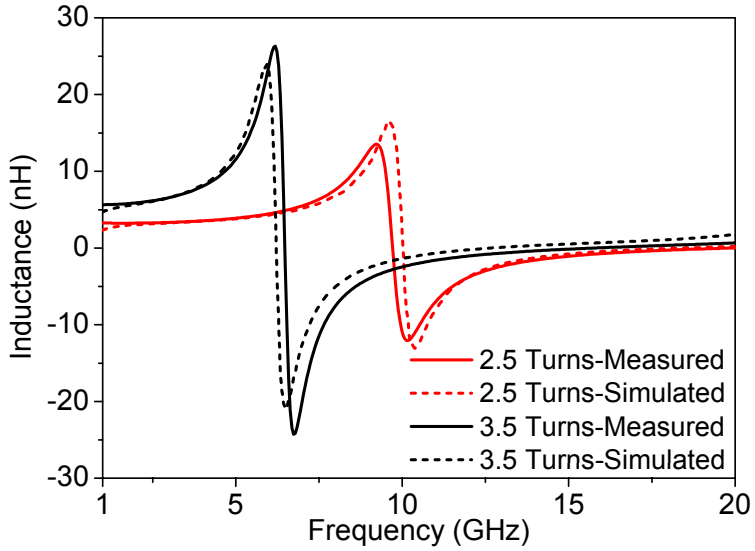




Measurement-Simulation Comparison II

- We extract the values of ε_r and tanδ of a PSi layer using a CPW
- We feed these values into HFSS to simulate the performance of inductors:
  - 2.5 turns – 3.2 nH
  - 3.5 turns – 6.1 nH
- We compare the simulations to the measurements of inductors fabricated on PSi having the used parameters

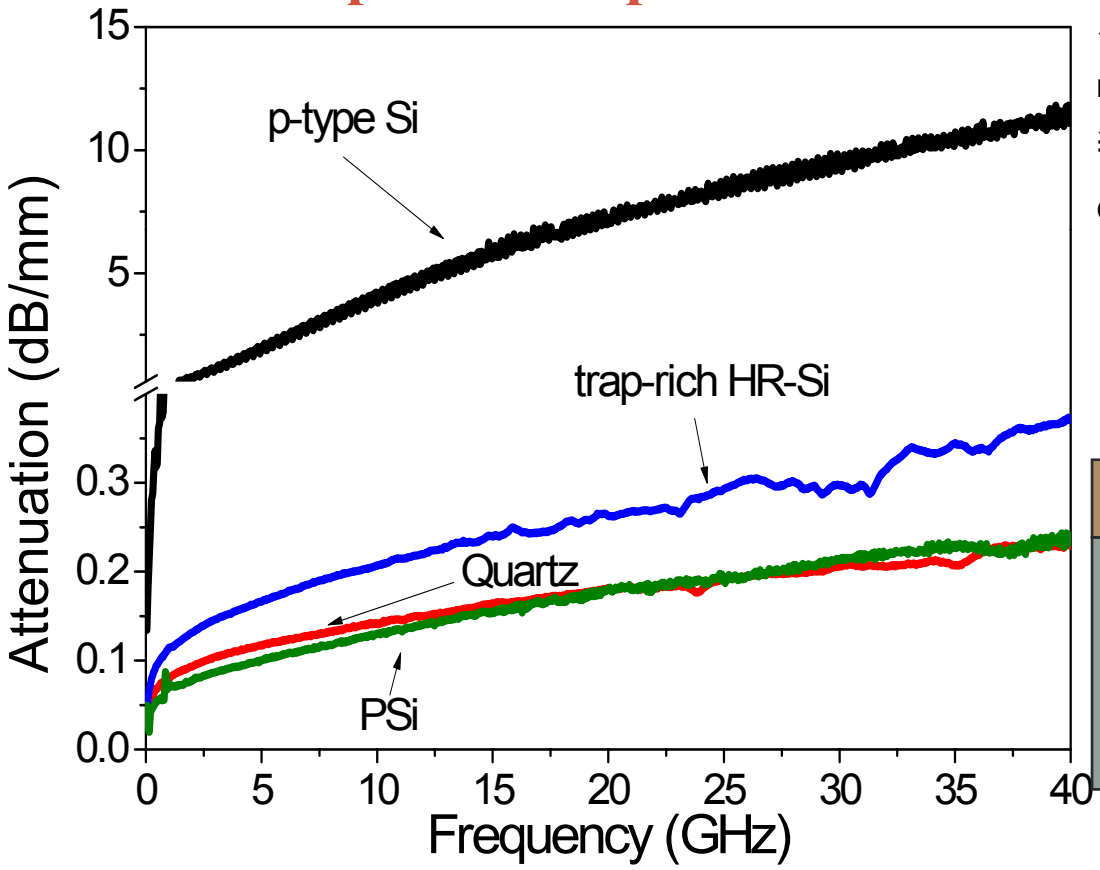


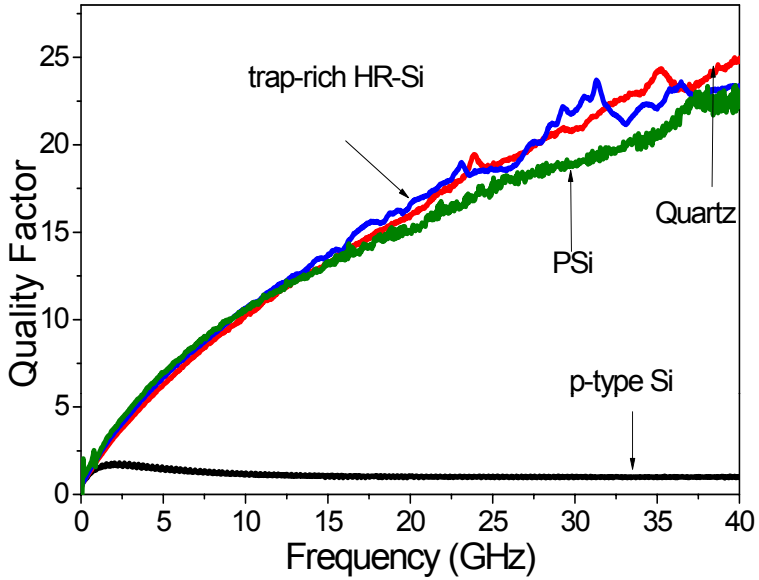


In order demonstrate the
effectiveness of porous Si as an RF substrate
we compare it with
different **state-of-the-art substrates**

Comparison of Different Substrates

CPWs on four different substrates
Comparison of performance





Values for PSi @ 40 GHz

α= 0.2 dB/mm
Q= 25
Z_C=90Ω
ε_{eff}=1.5

Comparable to quartz substrate ! (off-chip)

Sarafis, P., Hourdakis, E., Nassiopoulou, A. G., Roda Neve, C., Ben Ali, K., & Raskin, J.-P. Solid-State Electron., 87, 27–33, (2013)

Conclusions

- A **method to accurately extract** the dielectric parameters of porous Si has been developed. Its **validity** has been proven
- **Very good agreement** between simulation and measurement for TLines and inductors has been obtained
- A **comparison** between porous Si and other state-of-the-art substrates for RF was made. The **superiority of porous Si** has been shown
- The developed method for RF extraction opens the possibility of **using commercial simulation programs to accurately design RF devices on porous Si**

Thank you for your attention!

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