Novel Low Temperature 3D Wafer Stacking Technology for High Density Device Integration

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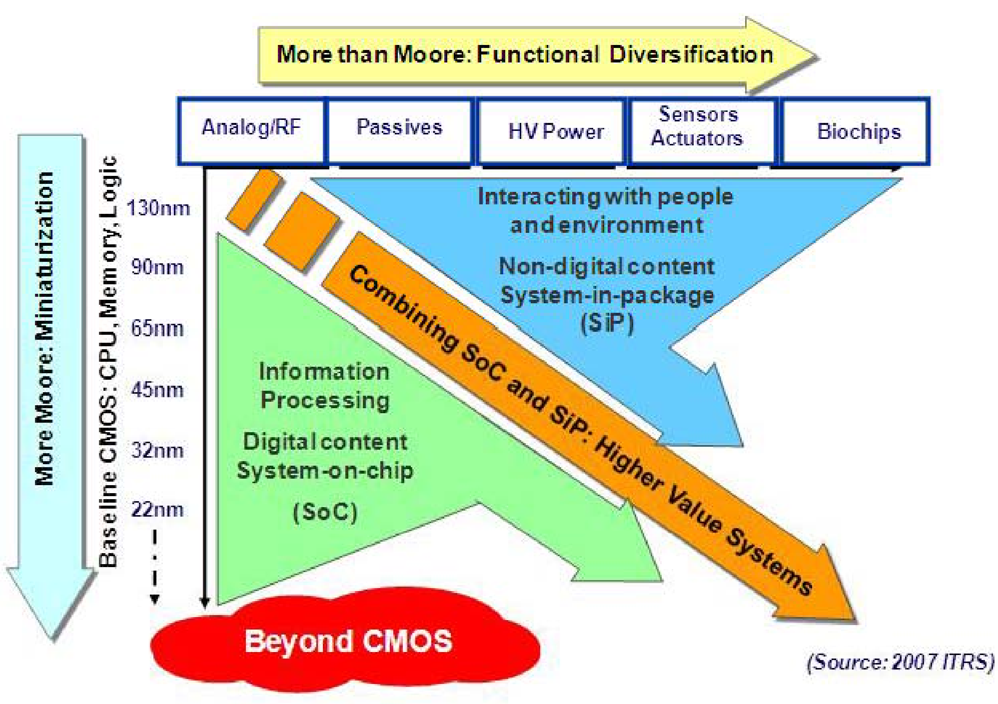
Outline

- 3D integration
- Low temperature layer stacking technology & requirements
- Electrical data
- Conclusions and outlook

Evolution of Device Technologies



- Scaling alone does not ensure improvement

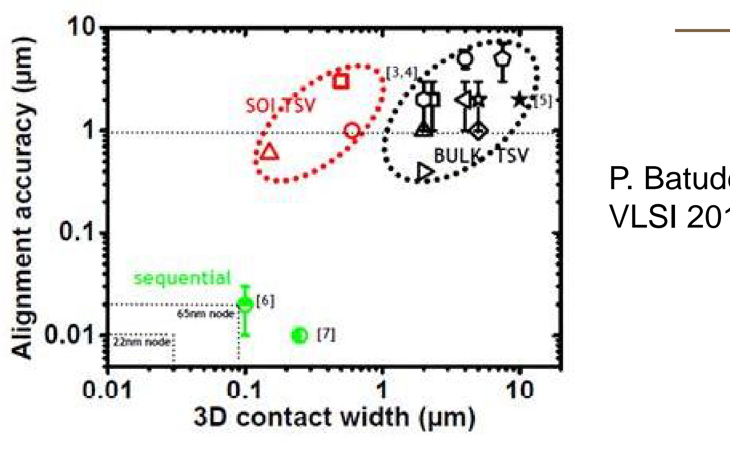
Towards a 3D world…

➔ Non-planar architectures (e.g. FinFET, GAA, etc)

➔ Heterogeneous integration

3D integration

Value for Electronic Systems	
Performance	↗
Density	↗
Functionality	↗
Form Factor	↘



P. Batude *et al.*
VLSI 2011

[3,4]: P.Garrou et al., Handbook of 3D integration, Vol 1,2 (Wiley ed) / [5]: B. Banijamali, ECTC2011
[6]: S-M. Jung et al., VLSI 2005 pp220 / [7]: P. Batude et al, ECS journal 2008, V016,pp47

- TSV based technology
  - Memory cube, etc

→ - Adoption delayed
- Reliability, yield and process cost challenges

- Sequential integration
  - Very dense device integration (nm alignment)

- Front End integration

Front End integration exemples

Examples	Applications	Source
Vertical transistors	Logic	Intel: K. Kuhn et al., TED 59:7 2012
Vertical transistors	Memory	[Toshiba, IEDM 1989] [Samsung, VLSI 2009] [Qimonda, Patent 2010]
Planar transistors	Logic	*CEA-LETI: P. Batude et al. VLSI 2011* **Alignment performance**: **~10nm** **3D contact process**: **planar scheme like**

3D layer stacking: concept

Low temperature Smart Cut™ for tranfer of blanket or predefined thin film stacks

SiGe, Ge, n^+, p^+ or undoped Si, III-V…

dielectrics, metals, silicides

Single crystalline films

Partially or fully processed wafers: e.g. CMOS, DRAM, etc

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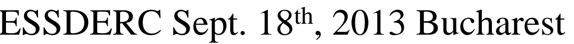
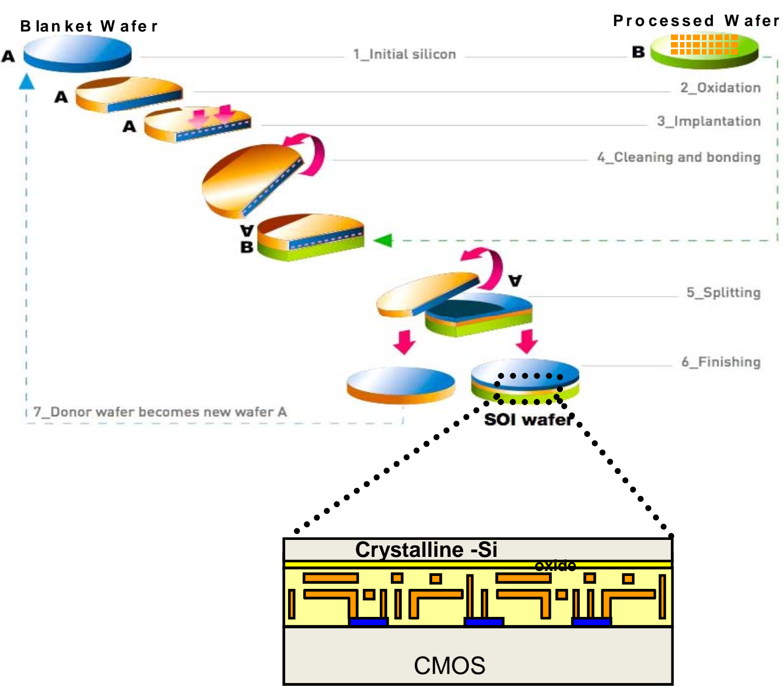


Low temperature Smart Cut^{TM}: Building blocks

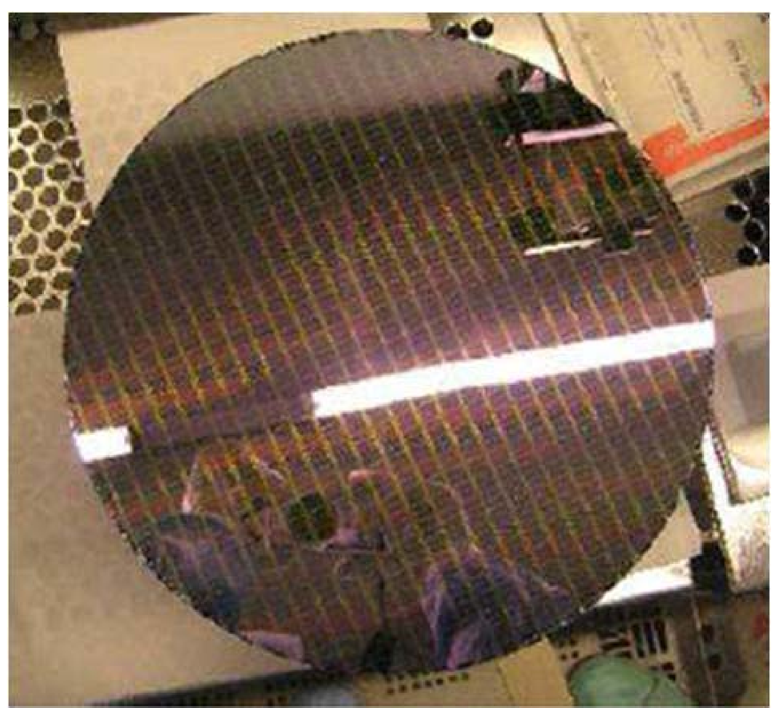
- Hydrogen implantation
- Pre-bond planarization and surface preparation
- Wafer direct bonding
- Low temperature layer splitting and finishing (<500°C)



➔ High quality thin films after low temperature layer transfer

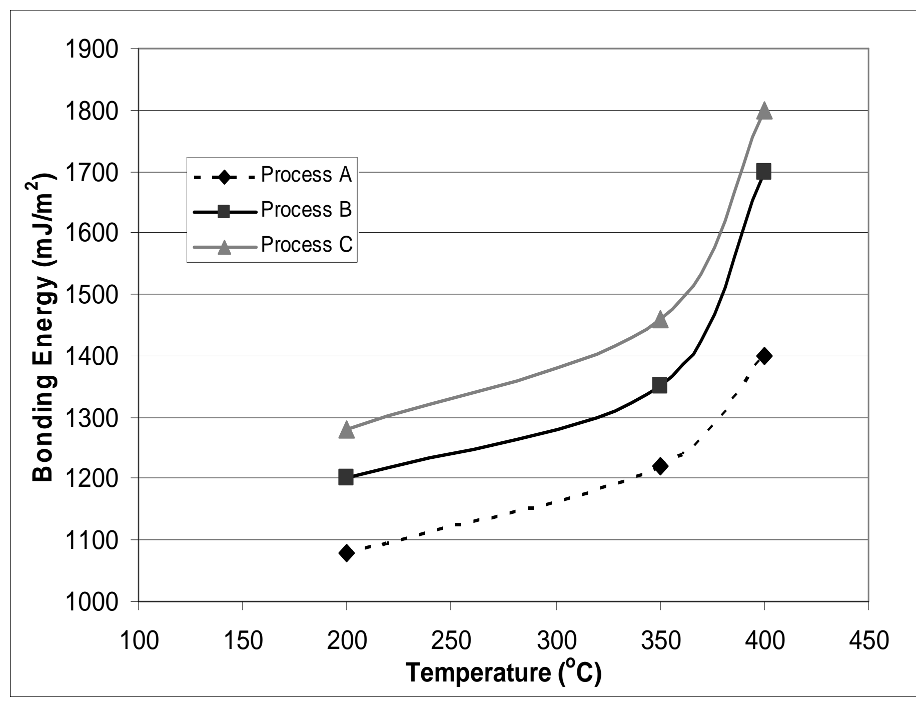
Low temperature Smart Cut^{TM}

- Thin Si layer transfer demonstrated on patterned wafers
  - Memory/Logic patterned substrate
  - 200nm ± 15nm top silicon layer
  - T_{max} < 500°C



300mm wafer

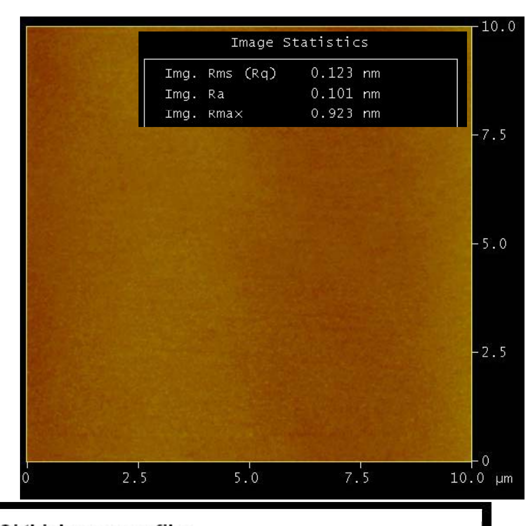
Surface conditioning before bonding allows low temperature interface consolidation

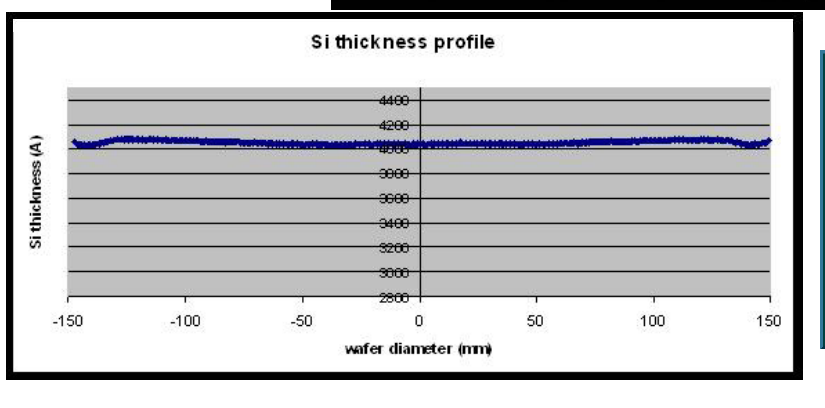


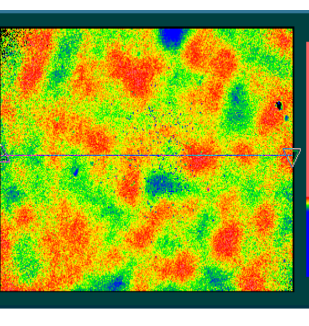
M. Sadaka, I. Radu, C. Lagahe-Blanchard and L. Di Cioccio, Cost Efficient Wafer-Level Stacking Technologies - Chip Scale Review Jan/Feb 2013

Low temperature Smart Cut^{TM} : finishing

- Physical characterization







☑ **Uniform thin Si film with low roughness**

L. Di Cioccio et al., *Wafer Level 3D Stacking using Smart Cut^{TM} and Metal-Metal Direct Bonding Technology*, ECS 2012

Outline

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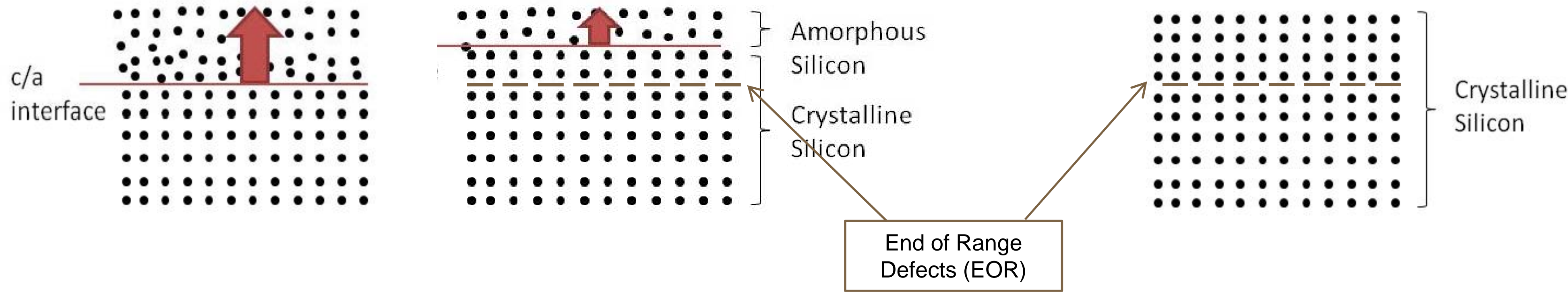
Low temperature activation of dopants

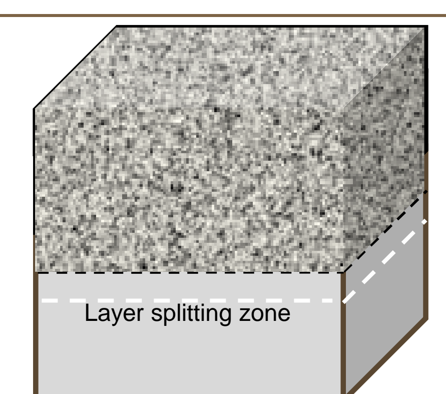
- Solid Phase Epitaxial Re-growth (SPER)
- Use crystalline silicon as a template to re-crystallize an amorphous silicon
- Annealing temperatures > 475°C
  (see Olson'94, E_a=2.7eV)

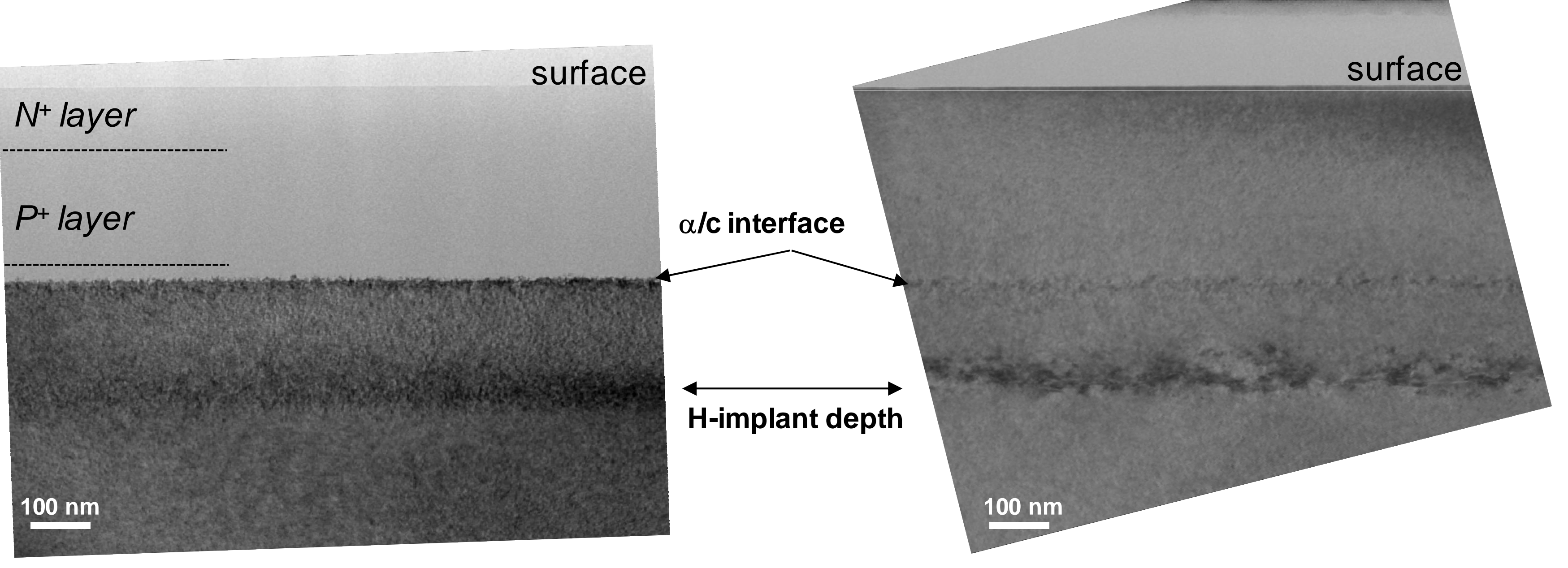


Key attribute:
➔ Activate doping impurities above solubility limit
(e.g. ultra shallow junction in the source/drain extension (SDE)

Low temperature SPER

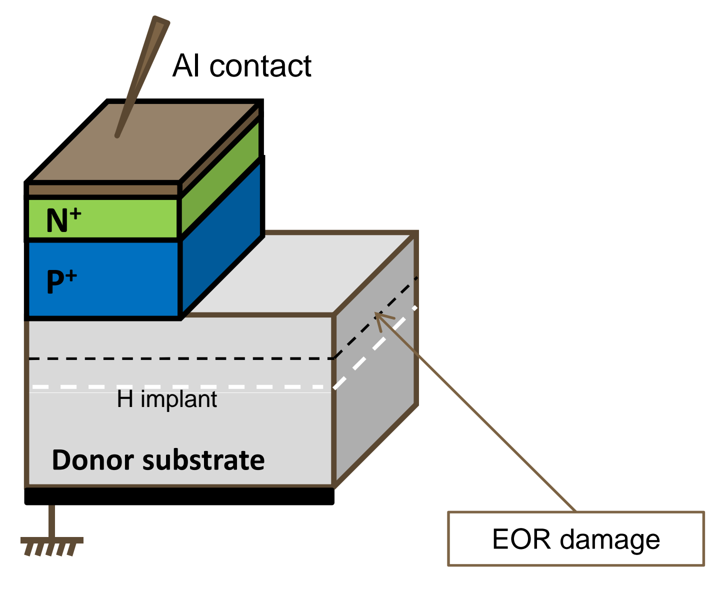
- Impact on PN thin film junction
  - H implantation (low dose - no layer transfer)
  - Si amorphization and subsequent re-crystallization at 500°C

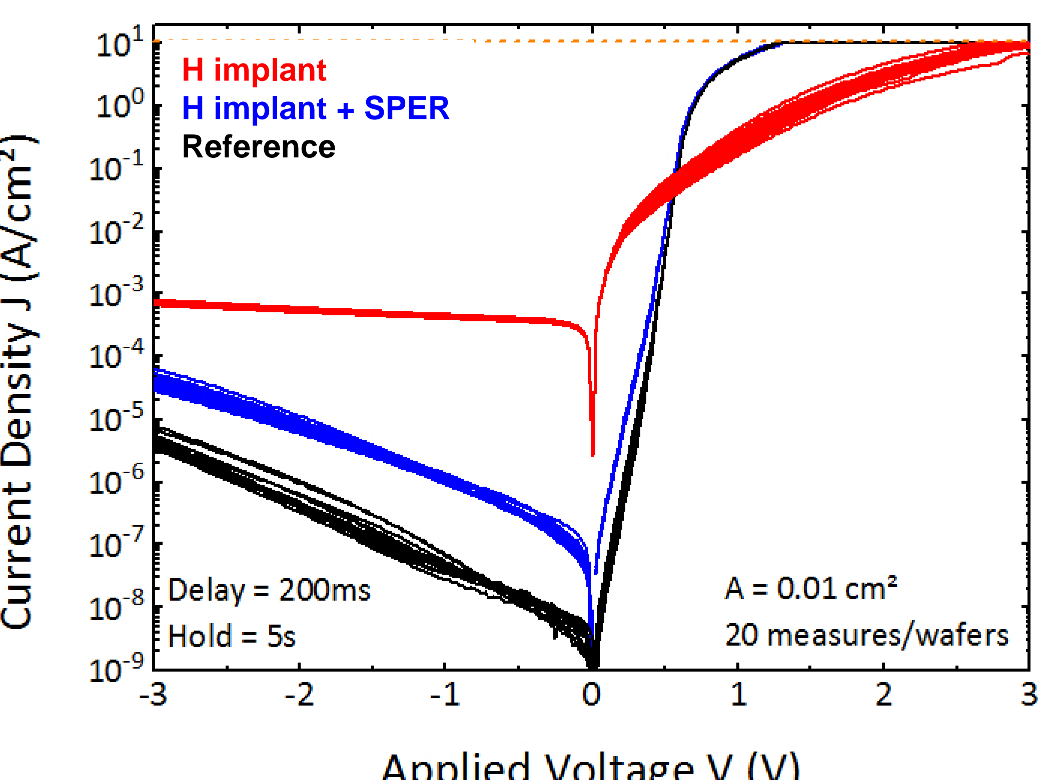




Low temperature SPER (500°C)

- I-V measurements





- PN diode recovery by low temperature SPER
- Higher I_{off} after re-crystallization due to subsisting EOR damage (Shockley-Read-Hall carrier generation)

Low temperature Smart Cut^{TM} and SPER

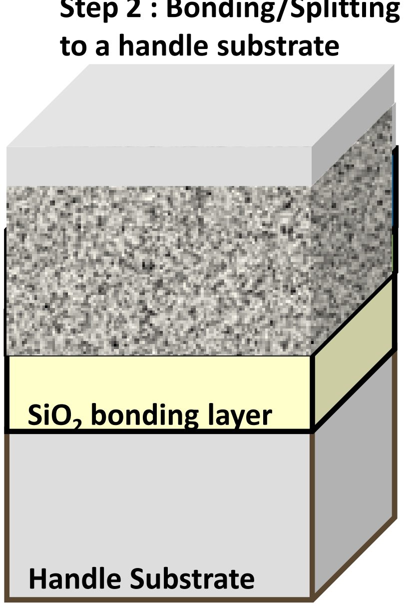
- Smart Cut and SPER integration leading to leakage free devices
  - Si amorphization before bonding
  - Bonding and layer splitting
  - Low temperature re-crystallization (SPER) $\leq$ 500°C
  - Thinning to removal of un-necessary Si material (including EOR defects)

Step 1 : Amorphization of active device layer

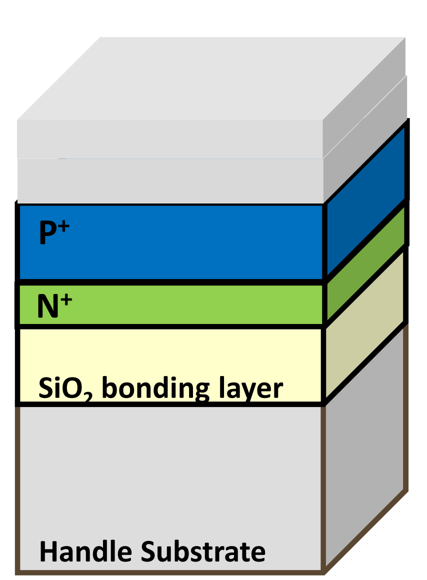
Layer splitting zone

Donor substrate

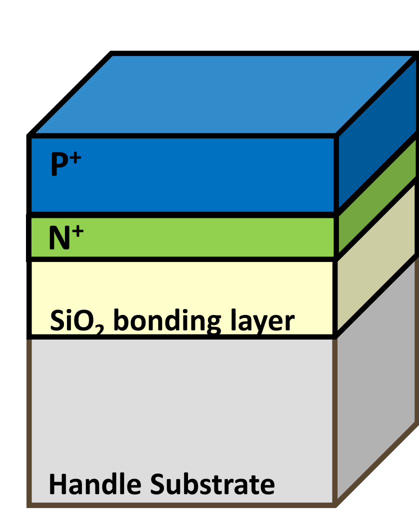
Step 2 : Bonding/Splitting to a handle substrate



Step 3 : low temp SPER

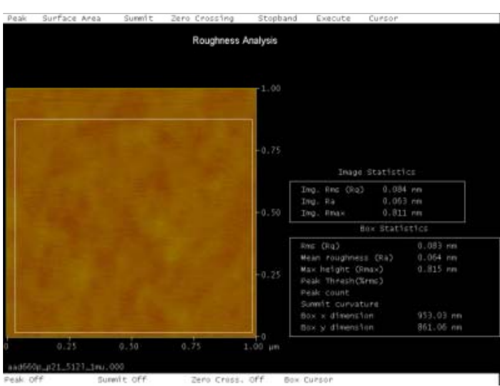


Step 4 : Thinning and finishing

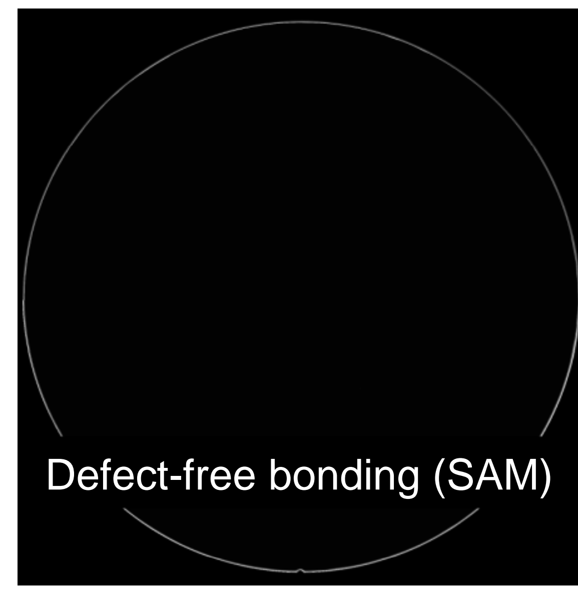


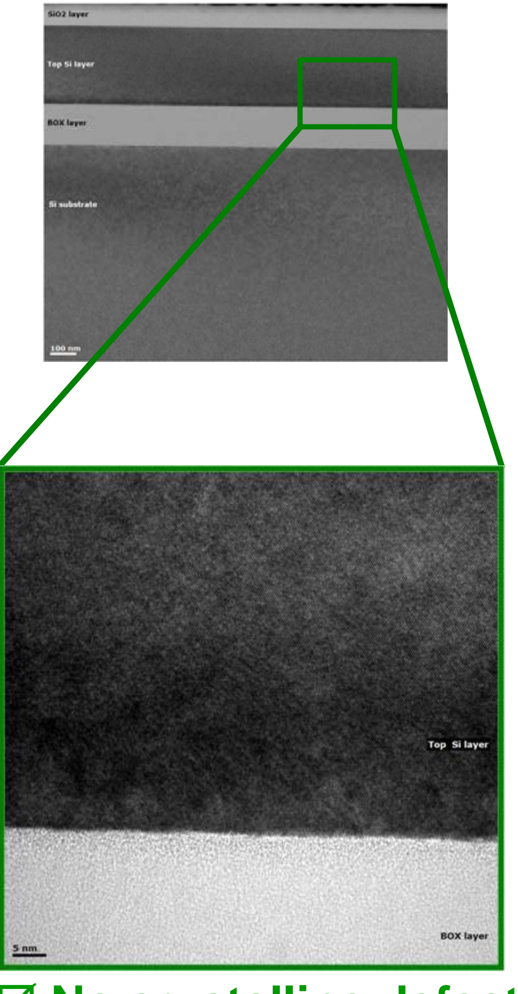
Low temperature Smart Cut^{TM} and SPER

- Validation using blanket Si film



☑ **low roughness of a-Si**

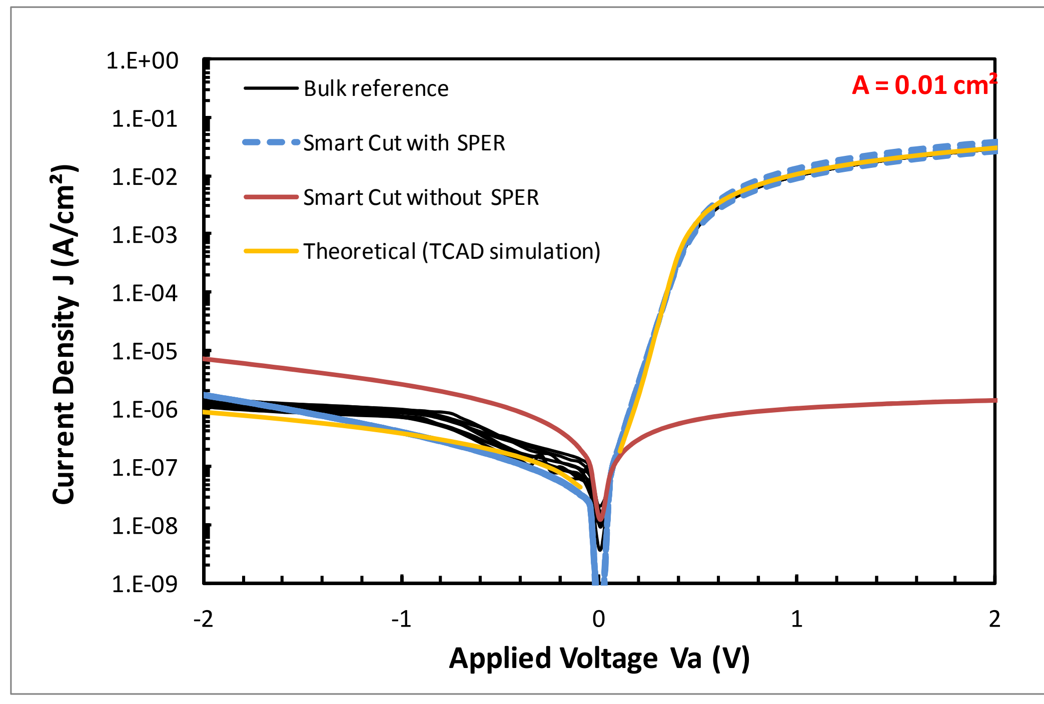


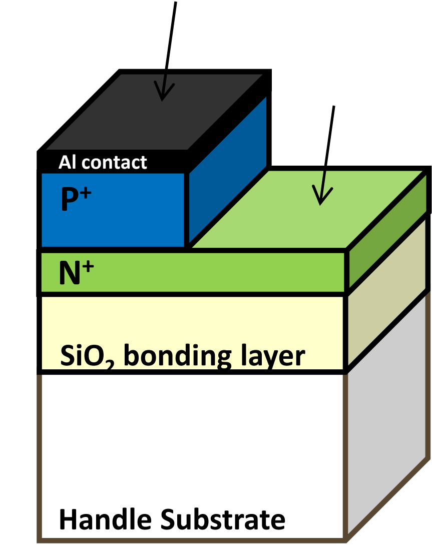


☑ **No crystalline defects**

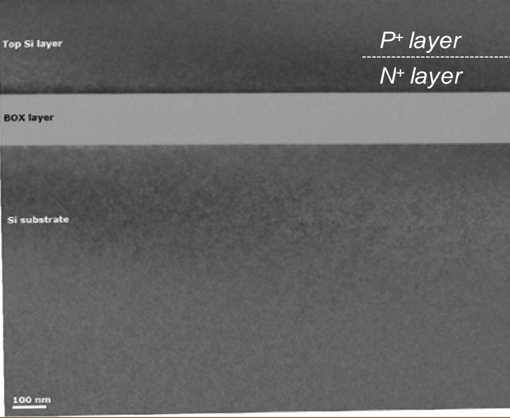
Electrical properties

- Smart Cut^{TM} and low temperature SPER integration leading to **defect free diode**
  - Validation using PN junction
  - 100% recovery of I(V) diode characteristics



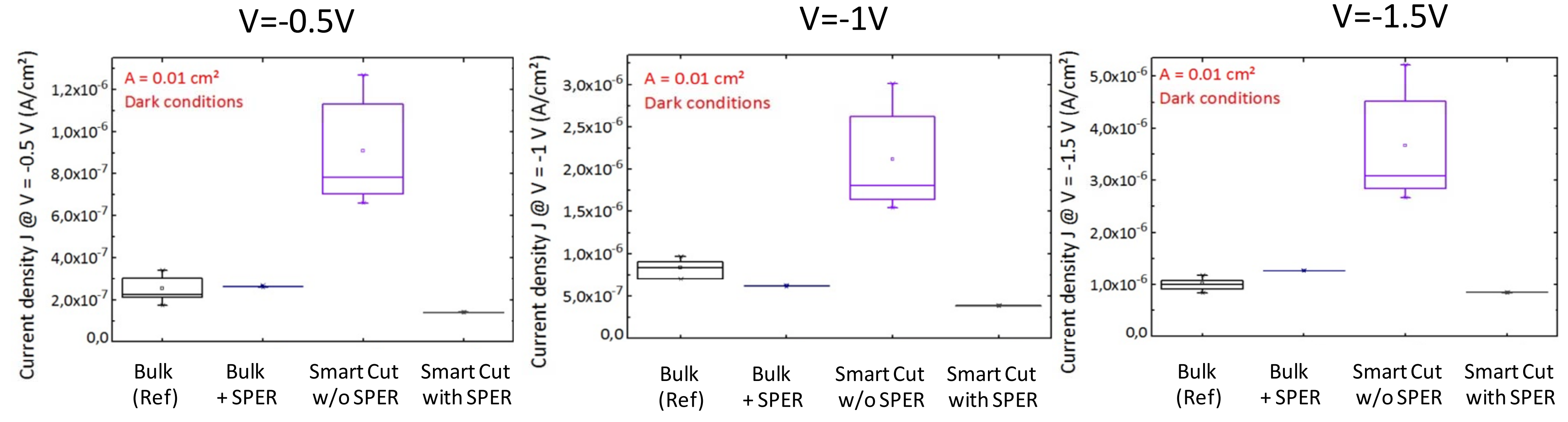


No degradation of I_{off}/I_{on} characteristics



Electrical properties

- Reverse current analysis under various polarization conditions



➔ Smart Cut with SPER integration leads to lowest I_{off}
➔ Lowest variability (statistical distribution)

Conclusions

- A novel 3D layer stacking technology at wafer level for very dense device integration is presented
- Successful layer transfer of high quality single-crystal silicon PN bi-layers using the Smart Cut^{TM} technology in combination with low temperature SPER
- Minimum diode leakage is demonstrated after the PN layer transfer without exceeding 500°C

Outlook

- Low temperature layer stacking enables front end integration of a large variety of devices
  - e.g. CMOS + memory blocks, CMOS + RF, CMOS + photonic interconnects, etc
  - Vertical or planar device integration schemes
  - Low temperature process compatible with pre-existing metallization
  - Wafer level path to monolithic 3D integration
- Heterogeneous integration of pre-defined stacks on silicon technology (single-crystal layers)
  - Single-crystalline template for new devices with nanometer alignment capability (standard lithography process)