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CHAIR'S MESSAGE

On behalf of the Organizing Committees of ESSCIRC 2013, it is our pleasure to welcome you to the 39th European Solid-State Circuit conference. ESSCIRC 2013 runs in parallel to its sister conference ESSDERC 2013, covering all aspects of modern solid-state systems, circuits and devices at a single event. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts and circuits and system designers. As a participant at ESSCIRC and ESSDERC, you will have the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered and succeeded.

The conferences are to be held at the JW Marriott Bucharest Grand Hotel, conveniently situated downtown. The venue is located next to the Parliament Palace, the largest building in Europe and the second largest in the world, right after the Pentagon.

This year, a total of 245 submissions originating from 35 countries were received for ESSCIRC including 104 papers coming from Europe, 90 from Asia-Pacific and 47 from North-America. This is proof of the truly international nature of ESSCIRC. The Technical Program Committee with 130 recognized experts from academia and industry selected 97 papers for oral presentations in 25 sessions. Six plenary presentations common to ESSCIRC and ESSDERC, and three keynotes specific for each conference focusing on highly relevant topics were selected by the Technical Program Committees of both conferences and will be delivered by outstanding speakers. One session of invited papers and two joint ESSDERC/ESSCIRC sessions complete the program.

In addition to the conference programs, a pre-conference day with introductory tutorials and a post-conference day with workshops showcasing work currently being carried out by European research consortia will also be held.

For this year edition, we are honored to host a round table on "The Future of Semiconductor Industry in Europe" with the participation of high level representatives of the major microelectronic companies, research institutes, as well as the funding organizations in Europe. The round table will offer the

panelists the chance to share their views on the topics that ensure the strength and sustainability of the microelectronic industry in Europe.

A special workshop on semiconductor research state-of-the-art in Eastern Europe will take place in the last day of the conference. The workshop entitled ”Potential of Eastern European countries in Key Enabling Technologies” is intended to expose to the international community the Eastern European achievements and to facilitate new contacts for future collaboration.

We would like to thank the Steering Committee of ESSDERC/ESSCIRC for giving us the opportunity to organize this event.

The conference has been organized by members of the University ”POLITEHNICA” of Bucharest, ”Gheorghe Asachi” Technical University of Iasi, IMT Bucharest (National Institute for R&D in Microtechnologies) and Infineon Technologies Romania. We would like to thank the authorities of these institutions for their support and for allowing us to devote part of our time to the organization.

Last but not least, we would like to express our greatest appreciation to all the authors who submitted papers to the conference and to all delegates, tutorial lecturers and plenary speakers who have travelled to Bucharest to interact and share their thoughts during the conference.

Enjoy ESSDERC/ESSCIRC 2013 conference and your visit to Bucharest. We hope to see you all back here more often.

Welcome, Bine ați venit!

Michael Neuhäuser
Conference Chair – ESSDERC/ESSCIRC 2013

Andrei Vladimirescu, Liviu Goras
TPC chairs – ESSCIRC 2013

University POLITEHNICA of Bucharest is the largest and the oldest technical university in the country and among the most prestigious universities in Romania. The tradition of this institution, developed in over 190 years through the effort of the most important nation's schoolmasters and of the generations of students, is not the only convincing reason. Today, the POLITEHNICA University of Bucharest is undergoing a continuous modernization process, being involved in a permanent dialogue with great universities in Europe and all over the world.

The Technical University „Gheorghe Asachi" Iaşi is among the oldest and prestigious academic institutions in Romania. It has a distinguished presence, both national and international, and it trains engineer professionals, able to quickly and efficiently respond to the innovation, research and development demands of the economic agents.

The University has the resources of intelligence and creativity as well as the skills required to generate, disseminate and implement the results of scientific approaches. Institution is working to strengthen a system of quality assurance and academic excellence in teaching and research.

The National Institute for R&D in Microtechnologies - IMT Bucharest, Romania (www.imt.ro) is supervised by the National Ministry of Education.

The field of activities corresponds to micro-nanosystems, micro-nanoelectronics and nanobio-technology. IMT – Bucharest was the first Eastern European institution promoting MST Technologies and a main performer in the region. Its European dimension is confirmed by its participation in the EU Frame Programs FP6 and FP7 (24 projects in ICT and NMP), FP7-related (11 projects: ENIAC-JU, MNT-ERANET, COST) and in national projects (ICT, Materials, Health, Security, Space).

Welcome to ESSCIRC 2013

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Infineon Technologies focuses on the three central challenges facing modern society: Energy Efficiency, Mobility and Security and offers semiconductors and system solutions for automotive and industrial electronics and chip card and security applications.

Infineon's products stand out for their reliability, their quality excellence and their innovative and leading-edge technology in analog and mixed signal, RF and power as well as embedded control.

With a global presence, Infineon operates through its subsidiaries in the USA from Milpitas, California, in the Asia-Pacific region from Singapore, and in Japan from Tokyo. In the 2012 fiscal year (ending September 2012), the company reported sales of 3.9 billion Euro.

Contents

ESSCIRC Schedule

Monday, September 16th, 2013

Tutorials

8:45 – 9:00	Opening
11:00 – 11:30	Morning coffee break
12:30 – 14:00	Lunch break
16:00 – 16:30	Afternoon coffee break
16:30 – 17:00 (17.30 - 18.00)	Wrap-up

Tuesday, September 17th, 2013

8:00	Conference Opening

Technical Sessions

8:30	Joint Plenary Lecture
9:20	Plenary Executive Round Table
10:50	Joint Plenary Lecture
11:40	Lunch
13:00	ESSCIRC Keynote
14:00	ESSCIRC Sessions
15:20	Coffee Break
15:50	ESSCIRC Sessions
16:50	ESSCIRC Sessions

Welcome Reception

Wednesday, September 18th, 2013

Technical Sessions

8:30	Joint Plenary Lecture
9:25	Joint Plenary Lecture
10:20	Coffee Break
10:50	ESSCIRC Sessions
12:30	Lunch
14:00	ESSCIRC Keynote
15:00	ESSCIRC Invited Session
16:00	Coffee Break
16:30	ESSCIRC Sessions

Gala Dinner

Thursday, September 19th, 2013

Technical Sessions

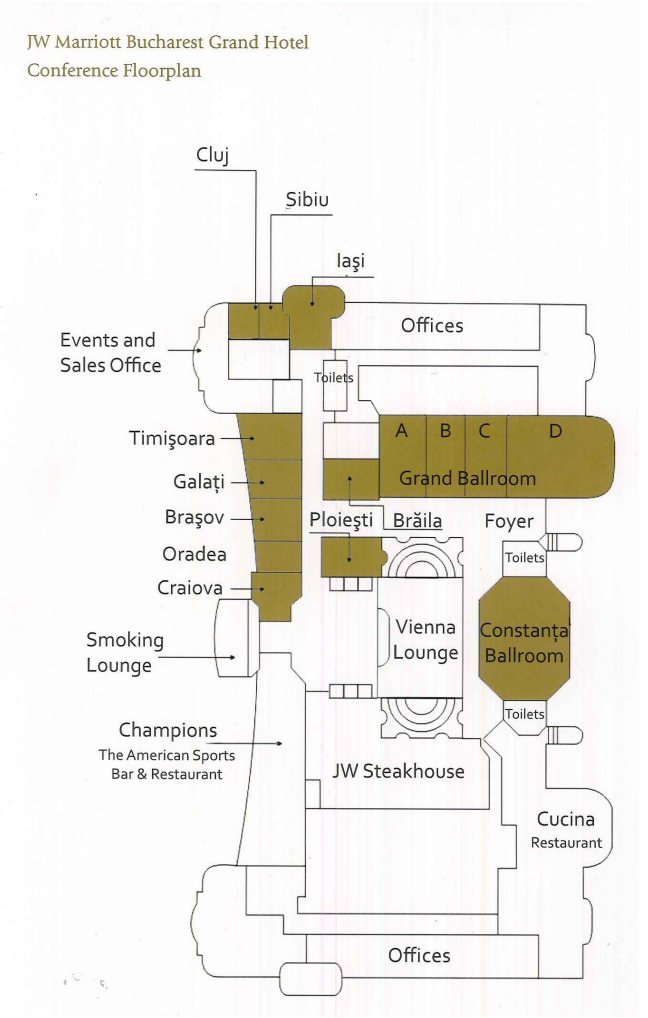
9:00	Joint Plenary Lecture
9:55	Joint Plenary Lecture
10:50	Coffee Break
11:20	ESSCIRC Keynote
12:20	Lunch
14:00	ESSCIRC Sessions
15:00	ESSCIRC Sessions
16:00	Coffee Break
16:20	ESSCIRC Sessions

Friday, September 20th, 2013

Workshops

8:50 (9:00) – 10:30	Work Session
10:30 – 11:00	Coffee Break
11:00 – 12:00	Work Session
12:00 – 13:30	Lunch
13:30 – 15:00	Work Session
15:00 – 15:30	Coffee Break
15:30 – 18:00	Work Session

Meeting Rooms Floorplan



Tuesday, September 17th, 2013

Time	Room A	Room B	Room C	Room D	Room C T	Room TM
08:00-08:30	**CONFERENCE OPENING** (Michael Neuhäuser, Conference Chair, Rakesh Kumar, IEEE SSCS President) (Room: ABCD)					
08:30-09:20	A1L-A **JOINT PLENARY**: Reinhard Ploss (Infineon) Chr: Michael Neuhaeuser Track: INVITED Joint Plenary (Room: ABCD)					
09:20-10:50	**Round Table: "Europe as Engine of Innovation in the Semiconductor Area"** (Room: ABCD)					
10:50-11:40	A2L-A **JOINT PLENARY**: Witek Maszara (Global Foundries) Chr: Andrei Vladimirescu Track: INVITED Joint Plenary (Room: ABCD)					
11:40-13:00	**Lunch + Exhibition**					
13:00-14:00	A3L-A **Emerging FET Devices** Chr: Radu Sporea, Andreas Schenk Track: ESSDERC-Emerging Non-CMOS Devices & Technologies		A3L-C **GaN and NEMS** Chr: Gunnar Malm, Henryk Przewlocki Track: ESSDERC-Characterization, Reliability & Yield		A3L-E **ESSCIRC Keynote**: E. Candes (Stanford Univ.) Chr: Boris Murmann Track: INVITED ESSCIRC	A3L-F **Emerging FET-like Modeling** Chr: Bernd Meinerzhagen, Wladek Grabinski Track: ESSDERC-Modeling & Simulation
14:00-15:20		14:20-15:20 A4L-B **Energy-Efficient High-Speed Circuits** Chr: Tobias Gemmeke, Doris Schmitt-Landsiedel Track: ESSCIRC-Digital Circuits	A4L-C **mmWave-to-THz Building Blocks and Systems** Chr: Yann Deval, Baudouin Martineau Track: ESSCIRC-RF & mm Wave		14:20-15:20 A4L-E **ESSDERC Keynote**: Tsunenobu Kimoto (Kyoto Univ.) Chr: Florin Udrea Track: INVITED ESSDERC	
15:20-15:50	**Coffee Break + Exhibition**					
15:50-16:50	A5L-A **PLLs** Chr: Francesco Svelto, Antonio Liscidini Track: ESSCIRC-RF & mm Wave	A5L-B **Innovation in Digital Circuit Architectures** Chr: Hannu Tenhunen, Christian Piguet Track: ESSCIRC-Digital Circuits			A5L-E **ESSDERC Invited Session I** Chr: Gunnar Malm Track: INVITED ESSDERC	
16:50-18:50	A6L-A **Analog I** Chr: Marco Berkhout, Traian Visan Track: ESSCIRC-Analog Circuits	A6L-B **Nyquist Rate ADCs** Chr: Georgi Radulov, George Gielen Track: ESSCIRC-Data Converters	A6L-C **Biomedical Circuits & Systems** Chr: Andreas Demosthenous, Firat Yazicioglu Track: ESSCIRC-Bio-Medical & Bio-Electronic Circuits & Systems	A6L-D **Power Converters and Drivers** Chr: Bernhard Wicht, Michael Mark Track: ESSCIRC-Power Management & Energy Scavenging	A6L-E **Technologies and Devices for RF and Power Applications** Chr: Gaudenzio Meneghesso, Gianmauro Pozzovivo Track: ESSDERC-Microwave & Power Solid State Devices	A6L-F **Optoelectronic and Photonic devices** Chr: Ion Tiginyanu Track: ESSDERC-Optoelectronic & Photonic Devices
20:00-23:00	**Welcome Reception at Hilton**					

Wednesday, September 18th, 2013

Time	Room A	Room B	Room C	Room D	Room C T	Room TM
08:30-09:25	B1L-A **JOINT PLENARY**: Wilfried Haensch (IBM) Chr: Adrian Ionescu Track: INVITED Joint Plenary (Room: ABCD)					
09:25-09:35	**Best Paper Awards ESSCIRC/ESSDERC-2012**					
09:35-10:30	B2L-A **JOINT PLENARY**: Stefan Finkbeiner (Bosch) Chr: Franz Dielacher Track: INVITED Joint Plenary (Room: ABCD)					
10:30-10:50	**Coffee Break + Exhibition**					
10:50-12:30	B3L-A **RF Receivers and Front-ends** Chr: Marc Borremans, Paul Muller Track: ESSCIRC-Wireless & Wireline Communication Circuits & Systems	B3L-B **Memories** Chr: Sylvain Clerc, Ralph Hasholzner Track: ESSCIRC-Processors, Memories & Interfaces	B3L-C **Magnetic, Temperature and Pressure Sensors** Chr: Hanspeter Schmid, Werner Brockherde Track: ESSCIRC-Sensors, Imagers & MEMs	B3L-D **Frequency Synthesis** Chr: Pietro Andreani, Jan Crols Track: ESSCIRC-RF & mm Wave	B3L-E **ESSDERC Keynote**: Livio Baldi (Micron) Chr: Raluca Muller Track: INVITED ESSDERC	
12:30-14:00	**Lunch + Exhibition**					
14:00-15:00	B4L-A **Emerging Devices** Chr: Francois Andrieu, Nadine Collaert Track: ESSDERC-Advanced CMOS Devices	B4L-B **Processing & Integration** Chr: Per-Erik Hellström, Simon Deleonibus Track: ESSDERC-Processing & Integration	B4L-C **Emerging Memories I** Chr: Andrea L. Lacaita, Dimitris Tsoukalas Track: ESSDERC-Advanced & Emerging Memories	B4L-D **Reliability Aspects from Device to Circuit I** Chr: Paolo Pavan Track: ESSDERC-Characterization, Reliability & Yield	B4L-E **ESSCIRC Keynote**: B. Murman (Stanford Univ.) Chr: Andrea Baschirotto Track: INVITED ESSCIRC	
15:00-16:00	B5L-A **Si-based Devices** Chr: Maryline Bawedin Track: ESSDERC-Advanced CMOS Devices	B5L-B **Silicon Doping** Chr: Emmanuel Augendre Track: ESSDERC-Processing & Integration		B5L-D **Reliability Aspects from Device to Circuit II** Chr: Paolo Pavan Track: ESSDERC-Characterization, Reliability & Yield	B5L-E **ESSCIRC Invited Session on Emerging Technology** Chr: Edoardo Charbon Track: INVITED ESSCIRC	
16:00-16:30	**Coffee Break + Exhibition**					
16:30-17:50	B6L-A **Emerging MOS: Variability & Defects** Chr: Tibor Grasser, Ray Hueting Track: ESSDERC-Modeling & Simulation	B6L-B **Nanowire Electronics** Chr: Costin Anghel, Elena Gnani Track: ESSDERC-Emerging Non-CMOS Devices & Technologies	B6L-C **Emerging Memories II** Chr: Kazunari Ishimaru, Olivier Thomas Track: ESSDERC-Advanced & Emerging Memories	B6L-D **Application-specific Processors & Circuits** Chr: Stefan Rusu, Marian Verhelst Track: ESSCIRC-Processors, Memories & Interfaces	B6L-E **RF Transceiver Circuits** Chr: Jussi Ryynanen, Peter Baltus Track: ESSCIRC-RF & mm Wave	B6L-F **CMOS Image Sensors** Chr: Angel Rodriguez-Vazquez, Johannes Solhusvik Track: ESSCIRC-Sensors, Imagers & MEMs
18:00-19:00				**ESSCIRC '14 TPC meeting**	**ESSDERC '14 TPC meeting**	
20:00-24:00	**Gala Dinner** **Invited Speaker C. Bulucea: "Eastern Europe's Semiconductor Technology - Recollections and Projections"**					

Thursday, September 19th, 2013

Time	Room A	Room B	Room C	Room D	Room C T	Room TM
09:00-09:55	C1L-A **JOINT PLENARY**: M. Maharbiz (UC, Berkeley) Chr: Liviu Goras Track: INVITED Joint Plenary (Room: ABCD)					
09:55-10:50	C2L-A **JOINT PLENARY**: J. del Alamo (MIT) Chr: Dan Dascalu Track: INVITED Joint Plenary (Room: ABCD)					
10:50-11:20	**Coffee Break + Exhibition**					
11:20-12:20	C3L-A **More than Moore** Chr: Steve Hall, Ryoichi Ishihara Track: ESSDERC-Emerging Non-CMOS Devices & Technologies	C3L-B **MEMS Devices and Technologies I** Chr: Mart Graef Track: ESSDERC-MEMS, Bio-sensors & Display Technologies		C3L-D **Advanced Characterization of Novel MOS FET Structures** Chr: Henryk Przewlocki, Gunnar Malm Track: ESSDERC-Characterization, Reliability & Yield	C3L-E **ESSCIRC Keynote**: P. Kinget (Columbia Univ.) Chr: Peter Mole Track: INVITED ESSCIRC	
12:20-14:00	**Lunch + Exhibition**					
14:00-15:00	C4L-A **Analog II** Chr: Boris Murmann, Hugo Veenstra Track: ESSCIRC-Analog Circuits	C4L-B **Oversampled ADCs I** Chr: Lucien Breems, Angelo Nagari Track: ESSCIRC-Data Converters	C4L-C **Millimeter-wave Circuits** Chr: Sven Mattisson, Peter Kennedy Track: ESSCIRC-Wireless & Wireline Communication Circuits & Systems	C4L-D **LED/LCD Drivers** Chr: Michiel Steyaert, Philip Mok Track: ESSCIRC-Power Management & Energy Scavenging	C4L-E **ESSDERC Keynote**: Kaustav Banerjee (UC, Santa Barbara) Chr: Max Lemme Track: INVITED ESSDERC	
15:00-16:00	C5L-A **Analog III** Chr: Peter Mole, Willy Sansen Track: ESSCIRC-Analog Circuits	C5L-B **Oversampled** ADCs II Chr: Claudius Dan, Piero Malcovati Track: ESSCIRC-Data Converters	C5L-C **Wake-up Receivers** Chr: Frank Op't Eynde, Jan Craninckx Track: ESSCIRC-Wireless & Wireline Communication Circuits & Systems	C5L-D **Voltage Regulators and Energy Harvesting** Chr: Marc Pastre, Patrick Reynaert Track: ESSCIRC-Power Management & Energy Scavenging	C5L-E **ESSDERC Invited Session II** Chr: Gheorghe Brezeanu Track: INVITED ESSDERC	
16:00-16:20	**Coffee Break + Exhibition**					
16:20-18:00	C6L-A **VCOs and Dividers** Chr: Andrea Bevilacqua, Alexandre Siligaris Track: ESSCIRC-RF & mm Wave	C6L-B **Circuits and Systems in Emerging Technologies** Chr: Eugenio Cantatore, Thierry Taris Track: ESSCIRC-Circuits & Systems in Emerging Technologies		C6L-D **Carbon-based Devices** Chr: Adrian Ionescu, Mircea Dragoman Track: ESSDERC-Carbon-based Devices	C6L-E **Emerging Memory Modeling** Chr: Cristell Maneux, An De Keetsgieter Track: ESSDERC-Modeling & Simulation	C6L-F **MEMS Devices and Technologies II** Chr: Piotr Grabiec Track: ESSDERC-MEMS, Bio-sensors & Display Technologies

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Welcome to Bucharest

The city of Bucharest is the capital of Romania and its most important cultural, business and financial center. A young and dynamic city, Bucharest has an eclectic architecture, which provides a view into its history. A mixture of medieval, neoclassical and Art Nouveau buildings, the city center also boasts recently built contemporary structures such as skyscrapers and office buildings. The city's majestic architecture and the sophistication of its elite earned Bucharest the nickname of "Little Paris" at the beginning of the 20th century.

Bucharest is easily accessible from all major European cities and with only one-stop connections from Asia and the Americas. The city benefits from a modern international airport and an extensive public transport system that is one of the largest in Europe.

Romania is the largest country in southeastern Europe and a member of the European Union since January 2007. The country is best known worldwide for its beautiful natural landscapes and UNESCO Heritage sites, such as The Danube Delta, the Monasteries of Moldova and the Transylvanian medieval cities. Also known as the mysterious land of the Legend of Dracula, Romania is a whole of fascinating experiences where Authentic, Natural and Cultural are the words that best capture its essence and make up an intriguing country rich in history, arts and scenic beauty.

The conference will be hosted in the upscale JW Marriott Bucharest Grand Hotel conveniently situated downtown. Inaugurated in 2000, the hotel exudes an essence of European elegance and comfort, providing excellent facilities for any large-scale event. The convention center includes 12 reconfigurable rooms adding up to a total of 2044 m2. The hotel is located next to the Parliament Palace, the largest building in Europe and the second largest in the world, right after the Pentagon.

Reaching "JW Marriott Bucharest Grand Hotel" by plane (approximately 1 hour):

When you arrive at Bucharest-Henri Coandă International Airport take the express Line 783 for 16 stations (aprox. 40 min) and get off at "Piața Unirii".

Then take the 385 bus for 6 bus stops (approx. 15 min) and get off at "Piața Arsenalului".

Conference Venue

Reaching "JW Marriott Bucharest Grand Hotel" from Downtown (approximately 30 minutes):

From "Universitate" bus stop (direction "Grădina Cişmigiu") take:

- bus 601, 163, 336 or
- trolleybus 61, 66, 69, 70, 85, 90, 91, 92.

Get off at "Grădina Cişmigiu"

Walk for 5 minutes to the "Elie Radu" bus station (near "Izvor" metro station). Take bus 385.

Stop at "Piaţa Arsenalului"

Language

The official language of the Conference is English

Webpages

ESSCIRC 2013 webpage: www.esscirc2013.imt.ro
ESSDERC 2013 webpage: www.essderc2013.imt.ro

Name Badges

All participants and accompanying persons are asked to wear their name badges in a visible place. Entrance to sessions is restricted to registered delegates only. Entrance to meeting halls and exhibition areas are granted to badge holders.

Speakers Briefing

Authors should meet their chairperson in the session room 15 minutes ahead the respective sessions.

Internet Access

Wireless internet access will be available at the conference venue without charge.

Conference Proceedings

All participants will receive an USB stick containing the accepted papers for both ESSCIRC and ESSDERC.

Best Paper Award

Papers presented at the conferences will be considered for the Best Paper Award and for the best “Young Scientist“ Paper Award. The selection will be based on the results of the paper selection process and the judgment of the chairmen. Award delivery will take place at ESSCIRC/ ESSDERC 2014.

Insurance Disclaimer

Participants are responsible for their own insurance. The organizers cannot take responsibility for any accident, loss or damage to participants or their property during the event.

Complaints

While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to rectify the issue.

Conference Overview

The aim of ESSCIRC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. ESSCIRC and ESSDERC (sister conference) are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts and circuits and system designers. While keeping separate Technical Program Committees, ESSCIRC and ESSDERC will share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

THEMES OF THE CONFERENCE

Analog Circuits

Amplification stages, Power amplifiers for audio, CT and DT filters, SC circuits, Comparators, Nonlinear circuits, Voltage/current references, HV circuits

Data Converters

Nyquist rate converters, Oversampled ADC and DAC, Sample-Hold circuits, ADC and DAC calibration/error correction circuits, Adaptative and smart data converters

RF and mm Wave

RF/IF/analog baseband circuits, LNAs, Mixers, Power Amplifiers, IF amplifiers, Power detectors, Modulators/demodulators, VCOs, PLLs, Frequency synthesizers, Frequency dividers, Integrated passive components

Wireless and Wireline Communication Circuits and Systems

Receivers/transmitters/transceivers for wireless systems, Base station and handsets, Advanced modulation systems, TV/radio/satellite receivers, Radars

Sensors, Imagers and MEMs

Sensor subsystems and interfaces, Accelerometers, Temperature sensing, Imaging and smart imaging chips, AMOLED, MEMs subsystems, RF MEMs

Digital Circuits

Digital circuit techniques, I/O and inter-chip communication, Reconfigurable digital circuits, Clocking, Arithmetic building blocks

Processors, Memories and Interfaces

Memories, Microprocessors, DSPs, Gigabit serial links, Clock and data recovery, Equalization, Memory interfacing, Bus interfacing, Multi-rate ICs

Bio-Medical and Bio-Electronic Circuits and Systems

Implantable electronic ICs, Bio-electronic integrated systems, Bio-medical imagers, Bio-MEMs integrated systems, Lab-on-chip, Wireless body area networks

Circuits & Systems in Emerging Technology

Digital, analog and mixed-signal circuits using emerging devices such as: Multigate MOSFETs, FinFETs, Flexible electronic components, Organic transistors, Nanowires/nanotubes, Quantum devices

Power Management and energy Scavenging

Energy transducers, Power regulators, DC-DC converters, LDOs, Boost converters, Buck converters, LED drivers, Sequencers and supervisors, Green circuits

Meals and Refreshments

All meals and refreshments will be served, for all the attendees, at scheduled times during the conference program, in Foyer Grand Ballroom and Restaurants (Cucina, Champions and JW Stakehouse)

SOCIAL PROGRAM

WELCOME RECEPTION, Tuesday, Sept. 17th

The Welcome Reception will take place on Tuesday evening at Athenee Palace Hilton, downtown Bucharest.

Transportation to the location will be provided. Bus departure from the conference venue (JW Marriott Bucharest Grand Hotel) will be at 19:00.

Return will be at 23:00 to conference venue (JW Marriott Bucharest Grand Hotel).

GALA DINNER, WEDNESDAY, SEPT. 18TH

The Gala dinner will be served on Wednesday evening at Ştirbey Palace.

Transportation to the location will be provided. Bus departure from the conference venue (JW Marriott Bucharest Grand Hotel) will be at 19:00.

Return will be from 23:00 to 24:00 to conference venue (JW Marriott Bucharest Grand Hotel).

Executive Round Table

The goal of the executive round table **"Europe as Engine of Innovation in the Semiconductor Area"** is to emphasize the strength and sustainability of the semiconductor industry in Europe. The choice of the event which embeds this plenary panel is far from being neutral; ESSCIRC-ESSDERC is the major meeting point of the semiconductor scientists in Europe. The distinguished panelists are (in alphabetical order):

- Jo De Boeck, Senior Vice President and Chief Technology Officer, IMEC, Belgium
- Thierry Collette, Vice President, LETI, France
- Philippe Magarshack, Executive Vice President, STMicroelectronics, France
- Lothar Pfitzner, Head of Semiconductor Manufacturing, Fraunhofer, Germany
- Reinhard Ploss, Chief Executive Officer, Infineon Technologies, Germany
- Hans Rijns, Chief Technology Officer, NXP Semiconductors, The Netherlands
- Andreas Wild, Executive Director, ENIAC Joint Undertaking, Belgium

The round table will be moderated by Andreia Cathelin, Senior Member of the Technical Staff, STMicroelectronics Crolles, and Jihad Haidar, Vice President and Managing Director, Infineon Technologies Romania.

Automotive electronics and energy efficiency

Dr. Reinhard Ploss, CEO Infineon

1. Semiconductors at the service of higher safety, more comfort, and low emission mobility (e.g. increased semiconductors in car for energy efficiency in engine, safety and body);

2. Semiconductors at the service of reduced emissions and a more efficient energy usage in the modern society (e.g. semiconductors in energy supply chain for higher efficiency);

3. What technologies are in place for different power/frequency/temperature etc… levels (e.g. Power Technologies roadmap, new materials etc.);

4. Innovation on technology (FE and BE) required to tackle the future challenges/bottleneck (our Power300 with thin wafer, new packages, system oriented thinking, etc.);

5. Examples with applications in automotive (Electric car) or Energy Grid showing the end user benefits (this can refer to components and/or technologies from Infineon).

Dr. Reinhard Ploss joined Siemens/Infineon in 1986, working in Munich as a process engineer with focus on chip manufacturing.

In 1992 he moved on to Villach, Austria, where he started in chip manufacturing and took over the position as Head of Technology in 1993. He returned to Munich in 1996 and took charge of the Power Semiconductor Business Unit, focusing on development and manufacturing. In 1999, Dr. Reinhard Ploss was appointed Head of the Industrial Power Business Unit as well as President of eupec GmbH Co. KG, a subsidiary of Infineon.

In 2000, Dr. Reinhard Ploss took over as President of the Automotive & Industrial Business Group of Infineon. From 2005 on, he held responsibility for manufacturing, development and operational management in the Automotive, Industrial & Multimarket Business Group.

In June 2007, Dr. Reinhard Ploss was appointed to the Management Board of Infineon, with responsibilities for manufacturing activities. In addition, he became Labor Director and Head of Research & Development. He remains responsible for these three areas to the present day.

Since October 1, 2012, Dr. Reinhard Ploss is Chief Executive Officer of Infineon Technologies AG.

FinFETs: Technology and Circuit Design Challenges

Witek Maszara, GLOBALFOUNDRIES

It took quarter of a century for multi-gate transistor to make it from first demonstration in research to a product – 22nm technology node microprocessor in 2012. FinFETs offer superior performance over incumbent planar devices due to their significantly improved electrostatics. FinFET technology faced two key barriers to their implementation in products: demanding process integration and its significant impact on layout and circuit design methodology. In this paper we focus on challenges and tradeoffs in both of these areas. Fin shape, pitch, isolation, doping, crystallographic orientation and stressing as well as device parasitics, performance and patterning approaches will be discussed. Implementation of high mobility materials for finFET devices will also be briefly reviewed as well as design challenges for logic and SRAM circuits.

Witold (Witek) P. Maszara has received MS degree in Electronics from Technical University of Wroclaw, Poland, and PhD degree from University of Kentucky in EE. Co-author of 100+ papers, author of over 50 invited talks and seminars, and over 60 patents in the field of microelectronics. Served as Technical Program Chair and General Chair of IEEE International SOI Conference, Chair of IEEE IEDM's Subcommittee for Integrated Circuits and Manufacturing . Currently serving on technical committees for IEDM and VLSI Symposium on Technology. Member of advisory boards for Semiconductor Research Corporation, Sematech, National Science Foundation, IMEC (Belgium) and INMP (Stanford U.) for broad range of semiconductor technology programs. Current areas of interest: CMOS logic technology, dense embedded memory and integrated photonics for deep submicron CMOS applications. He is presently employed at GLOBALFOUNDRIES as Principal Member of Technical Staff. Currently manages GLOBALFOUNDRIES Exploratory Research for 7nm technology node and beyond, covering Device, Interconnect, Memory and Photonics research.

Carbon Electronics - what can we do with it?

Wilfried Haensch, IBM

The slowdown of scaling intensified the search for the “next switch”. The dream is, of course, to find a new switching element that can replace the conventional transistor. Preferably without any change of the existing infra-structure – new materials and fabrication methods would be tolerated. Due to its superb thermal and electrical transport properties carbon in form of graphene or carbon nanotubes (CNTs) is considered as a natural successor of the current available technology solutions in the digital and RF space. In both, graphene and CNTs, devices can be build that resemble very closely the existing device structures and would therefore fit into the existing technology ecosystem without major interruptions. However, graphene and CNT based device technologies come with their own challenges that have to be overcome to insert them into a technology. I will discuss current progress in graphene and CNT device research and will provide insight in possible application spaces for these materials. A brief outlook is given on how graphene could be used for none conventional device architecture solutions.

Wilfried Haensch received his Ph.D. in 1981 from the Technical University of Berlin, Germany in the field of theoretical solid state physics. He started his career in Si technology 1984 at SIEMENS corporate research Munich. There he worked on high field transport in MOSFETs. In 1990 he joined the DRAM alliance between IBM and SIEMENS to develop quarter micron 64M DRAM. From there he moved in 1996 to INFINEON’s manufacturing facility in Richmond VA to be involved in the production of various generations of DRAM. In 2001 he joint IBM TJ Watson Research Center to lead a group for novel devices and applications. In this function he was responsible for the exploration of device concepts for 15nm node and beyond, new scaling concepts for memory and logic circuits, including 3D integration. He is currently responsible for post CMOS device solution and Si technology extensions. This includes carbon electronics for RF and digital applications and optical and electrical material properties of graphene and carbon nano tubes. He is the author of a text book on transport physics and author/co-author of more than 100 publications. He was awarded the Otto Hahn Medal for outstanding Research in 1983. He was named IEEE Fellow in 2012.

Nanometer-scale InGaAs Field-Effect Transistors for THz and CMOS technologies

Jesus A. del Alamo, MIT, USA

Integrated circuits based on InGaAs Field Effect Transistors are now widely used in the RF front-ends of smart phones and other mobile platforms, wireless LANs, high data rate fiber optic links and many defense and satellite communication systems. InGaAs ICs are also under intense research for new millimeter-wave applications such as collision avoidance radar and gigabit WLANs. In the last few years, as Si CMOS faces mounting difficulties to maintain its historical scaling path, InGaAs-channel MOSFETs have emerged as a credible alternative for mainstream logic technology capable of scaling to the 10 nm node and below. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. The intense research that this exciting prospect is generating will also reinvigorate the long march of InGaAs FETs towards the first true THz electronics technology. This talk will review progress and challenges of InGaAs-based FET technology for THz and CMOS.

Jesus A. del Alamo obtained a Telecommunications Engineer degree from the Polytechnic University of Madrid in 1980 and MS and PhD degrees in Electrical Engineering from Stanford University in 1983 and 1985, respectively. From 1985 to 1988 he was with NTT LSI Laboratories in Atsugi (Japan) and since 1988 he has been with the Department of Electrical Engineering and Computer Science of Massachusetts Institute of Technology where he is currently Donner Professor and MacVicar Faculty Fellow. His current research interests are centered on nanoelectronics based on compound semiconductors. He is also investigating the potential of online laboratories for science and engineering education.Prof. del Alamo was an NSF Presidential Young Investigator. He is a member of the Royal Spanish Academy of Engineering and Fellow of the IEEE. He currently serves as Editor of IEEE Electron Device Letters.

MEMS for automotive and consumer electronics

Stefan Finkbeiner, Bosch

MEMS, tiny micro-electro-mechanical systems that function as miniature machines, are showing up in all facets of our daily lives — Established in Automotive applications since almost 30 years, they can be found today predominantly in smartphones, tablets, cameras, laptops, video games! Your favorite consumer product likely contains more than a half-dozen MEMS. From accelerometers and gyroscopes that 'interpret' motion into the digital realm, to magnetic compasses, pressure sensors and MEMS microphones, MEMS sensors have dramatically improved the user experience with electronic devices.

Some of the addressed aspects:

- Current MEMS sensor context in smartphones & automotive.
- Evolution of use cases – introduction of new sensor types and addressing of new applications.
- The concept of Application Specific Sensor Nodes (ASSN's).
- How will the IoT emerging market impact or will be impacted by sensor node developments.

CEO and General Manager of Bosch Sensortec GmbH, **Dr. Stefan Finkbeiner** was born in 1966 in Freudenstadt, Germany. He received his Diploma in Physics from the University of Karlsruhe in 1992. He then studied at the Max-Planck-Institute in Stuttgart and received his PhD in Physics from the University of Stuttgart in 1995.

Dr. Finkbeiner joined Robert Bosch GmbH in 1995 and has been working for more than 17 years in different positions related to the research, development, manufacturing, and marketing of sensors. Senior positions at Bosch have included Director of Marketing for sensors, Director of Corporate Research in microsystems technology, and Vice President of Engineering for sensors.

Before joining Bosch Sensortec GmbH end of 2012 as CEO and General Manager he was the CEO of Akustica, a Bosch Group company which develops MEMS microphones for consumer electronics applications and is located in Pittsburgh, PA, USA.

Cyborg insects and other things: building interfaces between the synthetic and the multicellular

M. Maharbiz, University of California Berkeley

Michel M. Maharbiz is an Associate Professor with the Department of Electrical Engineering and Computer Science at the University of California, Berkeley.

He received his Ph.D. from the University of California at Berkeley for his work on microbioreactor systems under Professor Roger T. Howe (EECS) and Professor Jay D. Keasling (ChemE). His work led to the foundation of Microreactor Technologies, Inc. which was acquired in 2009 by Pall Corporation. From 2003 to 2007, Michel Maharbiz was an Assistant Professor at the University of Michigan, Ann Arbor. He is the co-founder of Tweedle Technologies, Cortera Neurotech and served as vice-president for product development at Quswami, Inc. from July 2010 to June 2011.

Prof. Maharbiz is a Bakar Fellow and was the recipient of a 2009 NSF Career Award for research into developing microfabricated interfaces for synthetic biology. His group is also known for developing the world's first remotely radio-controlled cyborg beetles. This was named one of the top ten emerging technologies of 2009 by MIT's Technology Review (TR10) and was in Time Magazeine's Top 50 Inventions of 2009. Dr. Maharbiz has been a GE Scholar and an Intel IMAP Fellow. Professor Maharbiz's current research interests include building micro/nano interfaces to cells and organisms and exploring bio-derived fabrication methods. Michel's long term goal is understanding developmental mechanisms as a way to engineer and fabricate machines.

Compressed Sensing

Emmanuel Candès, Stanford University

Emmanuel Candès is the Barnum-Simons in Mathematics and Statistics, and a Professor of Electrical Engineering (by courtesy) at Stanford University. He received his Ph.D. degree in statistics from Stanford in 1998. His research interests are in computational harmonic analysis, statistics, information theory, signal processing and mathematical optimization. He received several awards including the Alan T. Waterman Award -- the highest honor bestowed by the National Science Foundation which recognizes the achievements of scientists who are no older than 35, or not more than seven years beyond their doctorate. He has given over 50 plenary lectures at major international conferences.

Scaling analog and RF circuits

Peter R. Kinget, Columbia University

CMOS technology scaling has fueled tremendous progress in electronics and has brought about system-on-chip (SoC) products with a broad impact on society and economy. Technology scaling is very beneficial to increase the performance and density for digital signal processing, computation and memory. Analog circuits remain the critical interfaces to connect the digital cores of SoCs to the physical world and need to satisfy increasing performance demands. At the same time, designing analog functions with scaled devices and reducing supply voltages is getting progressively harder. Meeting more stringent performance requirements with poorer analog devices makes the task of the analog designer very challenging and interesting. We will review scaling challenges for analog circuit performance (Power, SNR, BW, Area) and contrast them to digital circuit scaling. We will further discuss design paradigms that address analog circuit scaling, including mixed-domain analog techniques. Recent examples illustrating the state of the art will be reviewed and prospects for future opportunities will be discussed.

Peter R. Kinget received the engineering and Ph.D. degrees in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1990 and 1996, respectively. From 1996 to 1999 he was a Member of Technical Staff at Bell Laboratories, Murray Hill, NJ. From 1999 to 2002 he held various technical and management positions in IC design and development at Broadcom, CeLight and MultiLink. He joined the faculty of the

Department of Electrical Engineering, Columbia University, NY in 2002 where he currently serves as a Professor. He is also a consulting expert on patent litigation and a technical consultant to industry.

His research interests are in analog, RF and power integrated circuits and the applications they enable in communications, sensing, and power management. He is widely published in journals and conferences, has co-authored 3 books and holds 11 US patents. Dr. Kinget is a Fellow of the IEEE. He has been a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society and an Associate Editor of the IEEE Journal of Solid State Circuits and the IEEE Transactions on Circuits and Systems II. He has served on the Technical Program Committees of the IEEE Custom Integrated Circuits Conference, the Symposium on VLSI Circuits, the European Solid-State Circuits Conference, and the International Solid-State Circuits Conference. He is currently an elected member of the IEEE Solid-State Circuits Society Adcom and a member of the Board of the Armstrong Memorial Research Foundation.

He is a co-recipient of the "Best Student Paper Award - 1st Place" at the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium; of the "First Prize" in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge; of the "Best Student Demo Award" at the 2011 ACM Conference on Embedded Networked Sensor Systems (ACM SenSys); of the "2011 IEEE Communications Society Award for Advances in Communication" for an outstanding paper in any IEEE Communications Society publication in the past 15 years; and of the "First Prize ($100K)" in the 2012 Interdigital Innovation Challenge (I2C).

Digitally-assisted data converter design

Boris Murmann, Stanford University

Modern CMOS technologies provide digital signal processing capabilities at high integration density and low energy per operation. Hence, expending digital signal processing to enhance performance-limiting analog building blocks has become a widely explored paradigm in modern ICs. In this talk, I will review the state-of-the-art in digitally assisted data converter design. The presentation will review the progress made over the past decade, evaluate the future prospects, and speculate about opportunities for long-term paradigm shifts.

Boris Murmann joined the Department of Electrical Engineering, Stanford, CA in 2004, where he currently serves

as an Associate Professor. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. From 1994 to 1997, he was with Neutron Mikrolektronik, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Dr. Murmann's research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. In 2008, he was a co-recipient of the Best Student Paper Award at the VLSI Circuits Symposium in 2008 and a recipient of the Best Invited Paper Award at the IEEE Custom Integrated Circuits Conference (CICC). He received the Agilent Early Career Professor Award in 2009 and the Friedrich Wilhelm Bessel Research Award in 2012. He currently serves as an Associate Editor of the IEEE Journal of Solid-State Circuits, the Data Converter Subcommittee Chair of the IEEE International Solid-State Circuits Conference (ISSCC) and as a program committee member of the European Solid-State Circuits Conference (ESSCIRC). He is an elected AdCom member of the IEEE Solid-State Circuits Society.

ESSCIRC Tutorials

Monday, Sept. 16, 2013

All tutorials are "Full-Day"

Circuit Design for Automotive

Organizer:

Franz Dielacher, *Infineon*

This tutorial day is dedicated to automotive electronics, encompassing the high voltage and high power technologies, complex system developments and robust circuit design required for automotive applications.

In the first presentation Herman Casier a retired engineering fellow from AMI Semiconductor will give a comprehensive overview on automotive- specific requirements and their impact on circuit design. The next two presentations will discuss design aspects for automotive applications. Bernhard Wicht from University Reutlingen will talk about smart-power IC's in high-voltage BiCMOS technologies and Dirk Hammerschmidt from Infineon will focus on integrated sensor design. The fourth paper will be presented by Jean-Michel Redouté from University Monash and will describe a structured approach to EMI resistant IC design. In the final presentation Georges Gielen from KU-Leuven will talk about modeling and design of analog circuits and how to make sure that they will function robust und reliable under all circumstances over the entire lifetime of the car.

Programme:

8.45 - 9.00	Opening
9.00 - 10.00	"Electronic circuits in an automotive environment" - Herman Casier, Consultant details
10.00 - 11.00	"Automotive Smart Power IC Design" - Bernhard Wicht, Uni Reutlingen details
11.00 - 11.30	Morning coffee break
11.30 - 12.30	"Integrated Sensors for Automotive Safety Applications" - Dirk Hammerschmidt, Infineon details
12.30 - 14.00	Lunch break
14.00 - 15.00	"A structured approach to EMI resistant IC design" - Jean-Michel Redouté, Monash University, Australia details

15.00 - 16.00	"Modeling and design of robust analog circuits" - Georges Gielen, KU Leuven, Belgium details
16.00 - 16.30	Afternoon coffee break
16.30 - 17.00	Wrap-up

Frequency Synthesis

Organizer:

R. Bogdan Staszewski, *TU Delft*

Frequency synthesizers are an integral part of all modern electronic devices, such as wireless/wireline communication and computational systems. This series of six tutorials cover various aspects of frequency synthesis ranging from RF to millimeter-wave frequencies, and for a wide range of applications: from mobile handsets and ultra low power nodes to basestation and microwave infrastructure.

Programme:

8.45 - 9.00	Opening
9.00 - 10.00	"Introduction and Landscape of Advanced Frequency Synthesizers" - R. Bogdan Staszewski, TU Delft details
10.00 - 11.00	"Frequency Synthesis for VSAT/P2P" - Domine Leenaerts, NXP details
11.00 - 11.30	Morning coffee break
11.30 - 12.30	"Ultra-low power PLL design for energy-efficient wireless applications" - Liu Yao-Hong, IMEC Holst Center details
12.30 - 14.00	Lunch break
14.00 - 15.00	"Flexible Clock Generation with Low Phase Error at High Power Efficiency" - Eric Klumperink, University Twente details
15.00 - 16.00	"Low-Voltage Transformer-Based CMOS VCOs and Frequency Dividers" - Howard Luong, Hong Kong University of Science and Technology details
16.00 - 16.30	Afternoon coffee break
16.30 - 17.30	"Integrated RF and mmWave CMOS Voltage Controlled Oscillators" - Andrea Mazzanti, University of Pavia details
17.30 - 18.00	Wrap-up

ESSCIRC Tutorials

Design solutions in nm CMOS

Organizer:

Andreia Cathelin, *STMicroelectronics*

This full day tutorials event addresses several of today's hot topics for the analog and RF designer: RF N-path filter design techniques, zero-energy smart sensor nodes, efficient time-interleaved analog to digital converters, low-power power converter design techniques and finally 3D heterogeneous integration by near field coupling. Distinguished professors from 3 continents will provide comprehensive high-level presentations, permitting to the audience to get good insight and major key points on the chosen topics.

Programme:

8.45 - 9.00:	Opening
9.00 - 10.00	"RF channel filtering: a revival of N-Path filters in Nanometer CMOS?" - Bram Nauta, Professor & Chair IC Design, University of Twente, The Netherlands details
10.00 - 11.00	"Zero-Energy Smart Sensor Nodes" - Jan M. Rabaey, Donald O. Pederson Distinguished Professor, University of California at Berkeley details
11.00 - 11.30	Morning coffee break
11.30 - 12.30	"Efficient Time-Interleaved Analog-to-Digital Converters" - Borivoje Nikolic, Professor, University of California, Berkeley details
12.30 - 14.00	Lunch break
14.00 - 15.00	"Low-Power Power Converter Design Techniques" - Philip Mok, Professor, Hong Kong Univ. of Sci. & Tech. (HKUST), Hong Kong details
15.00 - 16.00	"3D Heterogeneous Integration by Near Field Coupling" - Tadahiro Kuroda, Professor, Electrical Engineering, Keio University, Japan details
16.00 - 16.30	Afternoon coffee break
16.30 - 17.00	Wrap-up

Friday, Sept. 20, 2013

Potential of Eastern European Countries in Key Enabling Technologies

Organizer:

Ion Bogdan, *TU Iasi, Romania*

Full day Workshop (9:00 – 18:00)

The aim of the workshop is to offer scientists form East European countries an opportunity to meet and to present, on the occasion of ESSCIRC/ESSDERC, the main directions of research in the domain of microelectronics in their regions/countries. A special presentation will be made by Dr. Andreas Wild, executive manager of ENIAC JU. The speakers come from most of the East European countries and represent reputed research institutions and universities. The presentations and the discussions that will follow will reveal state-of-the-art of the research in East European countries and are intended to open new ways for a stronger cooperation between scientists working in the semiconductor domain.

Speakers at the workshop:

- Andreas Wild, Executive Director of the ENIAC Joint Undertaking
- Anelia Pergoot, ZMD Eastern Europe, Bulgaria
- Ion Tighineanu, Academy of Science, Moldova Republic
- Piotr Grabiec: Instytut Technologii Elektronowej (ITE), Warsaw
- Raluca Müller, National Institute for R&D in Microtechnologies (IMT Bucharest), Romania
- Aleksandr Korotkov, Sankt Petersburg State Polytechnical University, Russia
- Valentin Turin, TCAD- Educational and Research Lab. in Micro- and Nanoelectronics State University ESPC, Orel, Russia
- Volkan Ozguz, Nanotechnology Research and Application Center, Sabanci University, Turkey
- Istvan Barsony, Institute of Technical Physics and Materials Science, MFA, Budapest, Hungary

- Peeter Ellervee, Tallin University of Technology, Estonia
- Daniel Donoval, Slovak University of Technology, Bratislava, Slovakia
- Ashkhen Yesayan, Institute of Radiophysics and Electronics, NAS, Armenia

MOS-AK Compact Modeling Workshop

Organizers:

Wladek Grabinski, *MOS-AK Group*, **and Prof. Andrei Vladimirescu,** *R&D Scientific Coordinator*
Full day Workshop (9:00 – 18:00)

Par4CR Workshop on Cognitive Radio

Organizer:

Peter Baltus, *TU Eindhoven, The Netherlands*

Full day Workshop (9:00 – 18:00)

By the year 2020, mobile and wireless communications will play a central role in all aspects of European citizen's lives. Realization of this vision demands a major shift from the current concept of "anywhere - anytime" to a new paradigm of "any network - any device", with relevant content and context in a secure and trustworthy manner.

As more devices "go wireless" and human wireless networks proliferate at unprecedented speed more bandwidth and better use of the RF spectrum will be required to avoid future "wireless traffic jams". In this context the realization of cognitive radio (CR) is essential to meet the requirements of future wireless communication infrastructures. Software defined radio (SDR) should be a step on the path towards CR. For these reasons the European Universities and Industrial Companies organized a partnership in order to develop software defined radio architecture toward cognitive radio (Par4CR). This project is funded by EU and organized in the frame of Industry-Academia Partnerships and Pathways (IAPP). Par4CR brings together a consortium of seven major European players to perform a joint research programme and exchange knowledge on technologies crucial for the development of software defined radio and cognitive radio. The seven partners are from industry: NXP Semiconductors, France; IMST GmbH, Germany;

Catena Holding, the Netherlands and Sweden, and from academia: Eindhoven University of Technology, the Netherlands; ESIEE, France; TNO, the Netherlands and Institute of Electron Technology, ITE, Poland.

In the workshop final results from the Par4CR project will be presented together with views on the subject from leaders in this field. The workshop will present the last scientific results from the Par4CR project on different subjects related to the Cognitive Transceivers Technologies, including signal conversion, digital signal processing technologies, RF front-end and antenna design.

FP7 Variability and Reliability Showcase

Organizer:

Asen Asenov, *U Glasgow, UK*, **and Antonio Rubio,** *UPC Barcelona, Spain*

Full day Workshop (9:00 – 18:00)

i-RISC Workshop on Innovative Reliable Chip Designs from Unreliable Components

Organizers:

Valentin Savin, *CEA LETI, Grenoble, France,* **and Sorin Cotofana,** *TU Delft, The Netherlands*

Full day Workshop (9:00 – 18:00)

The ongoing miniaturization of data processing and storage devices and the imperative of low-energy consumption can only be sustained through low-powered components. However, lower supply voltages combined with variations in technological process of emerging nanoelectronic devices make them inherently unreliable. As a consequence, the nanoscale integration of chips built out of unreliable components has emerged as one of the most critical challenges for the next-generation electronic circuit design. To make such nanoscale integration economically viable, new solutions for efficient and fault-tolerant data processing and storage must be investigated.. Workshop Purpose: The i-RISC Workshop addresses the problem of reliable computing with unreliable components, which is a crucial issue for the long-term development of computing technology. The Workshop main goal is to explore the synergistic utilization of information and coding theory and techniques, traditionally utilized to improve the

reliability of communication systems, and circuit and system theory and design techniques in order to create reliable/predictable hardware. The aim is to enable the development of innovative fault-tolerant solutions at both circuit- and system-level that are fundamentally rooted in mathematical models, algorithms, and techniques of information and coding theory.

In the Quest for Zero Power: Enabling Smart Autonomous System Applications

Organizer:

Adrian Ionescu, *EPFL, Switzerland*

Full day Workshop (9:00 – 18:00)

Keynote

- The role of new materials in nanoelectronics – Robert Westervelt, Harvard University

Session 1: Smart Autonomous Systems

- Technology challenges for a smarter planet – Walter Riess, IBM Zürich
- Roadmaps for future nanolectronics – Denis Rousset, Catrene, Paris

Session 2: Ultra low power computation & communication

- Computing with NEMS –Hervé Fanet, CEA-LETI, Grenoble
- Graphene: an enabler of low power devices? Max Lemme, University of Siegen
- Tunnel FET versus MOSFET: a critical review – Giorgio Baccarani, University of Bologna

Session 3: Heterogenous integration

- The e-BRAINS project - Peter Ramm, Fraunhofer Research Institution for Modular Solid State Technologies EMFT, Munich
- Heterogeneous integration for infrared sensors, Adriana Lapadatu, SINTEF

Session 4: Low power sensors and energy scavenging for system integration

- Energy harvesting for self-powered sensor systems–

Rob van Schaijk, IMEC-NL

- Carbon-based sensors, Cosmin Roman, ETH Zürich
- Chemical sensors: towards the 6th sense system – Max Fleischer, Siemens
- Mechanical energy harvesiting– Eric Yeatman, Imperial College

Session 5: New opportunities in Horizon 202o for Smart Systems

- Priorities and funding strategies in Horizon 2020 for Smart Systems - Dirk Beernaert, European Commission - tbc

SINANO Workshop: "Nanowires for Logic, Memory and New Functionalities"

Organizer:
Francis Balestra, *Sinano Institute - Grenoble INP/ CNRS*

Full day Workshop (9:00 – 18:00)

This Workshop is supported by the European Institute of Nanoelectronics SINANO (www.sinano.eu) and aims at discussing state-of-the art results and disruptive achievements in the field of Nanowires for very low power and high performance logic and memory, and for adding new functionalities to CMOS in the More than Moore domain (sensing, energy harvesting, RF and e-cooling).

8:50	"Introduction", Francis Balestra, Sinano Institute
9:00	"Nanowire devices for the 10nm technology node and beyond", Sylvain Barraud, CEA-LETI -9:30 "Extending Moore's law: Nanowires to the rescue", Nadine Collaert, IMEC
10:00	"Energy efficient electronics: prospects and challenges of superlattice nanowire FETs", Elena Gnani, Giorgio Baccarani, IUNET-University of Bologna
10:30	Coffee break
11:00	"Complementary Strained Si nanowire TFETs and Inverters", Qing-Tai Zhao, Siegfried Mantl, Forschungszentrum Juelich

11:30	"Challenges and opportunities in InAs Tunnel FETs: a simulation study", Marco Pala, IMEP-LAHC, Grenoble INP/CNRS, David Esseni, IUNET-University of Udine
12:00-13:30	Buffet lunch
13:30	"Nanowires for sensing applications", Per-Erik Hellström, Mikael Ostling, KTH
14:00	"Piezoelectric nanowires for mechanical energy harvesting ", Gustavo Ardila, IMEP-LAHC, Grenoble INP-Minatec
14:30	"Nanowires and nanostructured Si for RF applications", Androula Nassiopoulou, IMEL/NCSR Demokritos
15:00	"e-cooling and impact of low dimensionality", Evan Parker, David Leadley, University of Warwick
15:30	**End of Workshop**

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Tuesday, September 17

ESSCIRC Keynote: E. Candes (Stanford Univ.)

Session Code: A3L-E

Location: Room CT

Date & Time: Tuesday, September 17
13:00 - 14:00

Chair(s): Boris Murmann
Stanford University

13:00 **Compressive Sensing: Principles and Hardware Implementations**
Emmanuel Candes[1], Stephen Becker[2]
[1]Stanford University, United States; [2]Universit Pierre et Marie Curie - Paris 6, France

Tuesday, September 17

mmWave-to-THz Building Blocks and Systems

Session Code: A4L-C

Location: Room C

Date & Time: Tuesday, September 17
14:00 - 15:20

Chair(s): Yann Deval
University of Bordeaux
Baudouin Martineau
STMicroelectronics

14:00 **A 19-dBm, 15-Gbaud, 9-bit SOI CMOS Power-DAC Cell for High-Order QAM W-Band Transmitters**
Stefan Shopov, Andreea Balteanu, Sorin P. Voinigescu
University of Toronto, Canada

14:20 **A 48 GHz 6-bit LO-Path Phase Shifter in 40-nm CMOS for 60 GHz Applications**
Chuang Lu[2], Marion Matters-Kammerer[2], Reza Mahmoudi[2], Peter Baltus[2], Ernst Habekotté[1], Koen van Hartingsveldt[1], Floris van der Wilt[1]
[1]Catena Microelectronics B.V., Netherlands; [2]Eindhoven University of Technology, Netherlands

14:40 **A 142GHz Fully Integrated Wireless Chip to Chip Communication System for High Data Rate Operation**
Samuel Foulon[2], Sébastien Pruvost[2], Denis Pache[2], Christophe Loyez[1], Nathalie Rolland[1]
[1]IEMN, France; [2]STMicroelectronics, France

15:00 **A 0.32 THz FMCW Radar System Based on Low-Cost Lens-Integrated SiGe HBT Front-Ends**
Konstantin Statnikov[1], Erik öjefors[2], Janusz Grzyb[1], Pascal Chevalier[3], Ullrich R. Pfeiffer[1]
[1]Bergische Universität Wuppertal, Germany; [2]Sivers IMA, Sweden; [3]STMicroelectronics, France

Tuesday, September 17

Energy-Efficient High-Speed Circuits

Session Code: A4L-B

Location: Room B

Date & Time: Tuesday, September 17
14:20 - 15:20

Chair(s): Tobias Gemmeke
IMEC
Doris Schmitt-Landsiedel
TUM

14:20 **Design Trade-Offs in Signal Component Separators for Outphasing Power Amplifiers**
Zhipeng Li, Yan Li, Yehuda Avniel, Alexandre Megretski, Vladimir Stojanovic
Massachusetts Institute of Technology, United States

14:40 **Power Sequence Free 400Mbps 90µW 6000µm² 1.8V-3.3V Stress Tolerant I/O Buffer in 28nm CMOS**
Vinod Kumar, Mohd. Rizvi
STMicroelectronics, India

15:00 **All-Digital Process-Variation-Calibrated Timing Generator for ATE with 1.95-ps Resolution and a Maximum 1.2-GHz Test Rate**
Kyungho Ryu, Dong-Hoon Jung, Seong-Ook Jung
Yonsei University, Korea, South

Tuesday, September 17

PLLs

Session Code: A5L-A

Location: Room A

Date & Time: Tuesday, September 17
15:50 - 16:50

Chair(s): Francesco Svelto
Univ. Pavia
Antonio Liscidini
University of Toronto

15:50 **A Supply-Noise-Rejection Technique in ADPLL with Noise-Cancelling Current Source**
Yusuke Niki, Daisuke Miyashita, Hiroyuki Kobayashi, Shouhei Kousai
Toshiba Corporation, Japan

16:10 **Wideband 2-16 GHz Local Oscillator Generation for Short-Range Radar Applications**
Michele Caruso[1], Matteo Bassi[2], Andrea Bevilacqua[1], Andrea Neviani[1]
[1]Università degli Studi di Padova, Italy; [2]University of Padova, Italy

16:30 **A 3.4mW 2.3-to-2.7GHz Frequency Synthesizer in 0.18-µm CMOS**
Chih-Hsiang Chang[1], Ching-Yuan Yang[2], Yu Lee[1], Jun-Hong Weng[3], Nai-Chen Cheng[1]
[1]Industrial Technology Research Institute, Taiwan; [2]National Chung Hsing University, Taiwan; [3]Tunghai University, Taiwan

Tuesday, September 17

Innovation in Digital Circuit Architectures

Session Code: A5L-B

Location: Room B

Date & Time: Tuesday, September 17
15:50 - 16:50

Chair(s): Hannu Tenhunen
KTH
Christian Piguet
CSEM

15:50 **A Fine Grain Variation-Aware Dynamic Vdd-Hopping AVFS Architecture on a 32nm GALS MPSoC**
Edith Beigne[1], Ivan Miro-Panades[1], Yvain Thonnart[1], Laurent Alacoque[1], Pascal Vivet[1], Suzanne Lesecq[1], Diego Puschini[1], Farat Thabet[2], Benoit Tain[2], Karim Benchehida[2], Sylvain Engels[3], Robin Wilson[3], Didier Fuin[3]
[1]CEA-LETI, France; [2]CEA-LIST, France; [3]STMicroelectronics, France

16:10 **MADmax: a 1080P Stereo-to-Multiview Rendering ASIC in 65 nm CMOS Based on Image Domain Warping**
Michael Schaffner[2], Pierre Greisen[2], Simon Heinzle[1], Frank Gürkaynak[2], Hubert Kaeslin[2], Aljoscha Smolic[1]
[1]Disney Research Zurich, Switzerland; [2]ETH Zürich, Switzerland

16:30 **A Flexible, Clockless Digital Filter**
Christos Vezyrtzis, Weiwei Jiang, Steven Nowick, Yannis Tsividis
Columbia University in the City of New York, United States

Tuesday, September 17

Analog I

Session Code: A6L-A
Location: Room A
Date & Time: Tuesday, September 17
16:50 - 18:50
Chair(s): Marco Berkhout
NXP
Traian Visan
Infineon

16:50 **A Four-Channel, ±36 V, 780 kHz Piezo Driver Chip for Structural Health Monitoring**
Yang Guo[2], Christopher Aquino[1], David Zhang[1], Boris Murmann[2]
[1]Acellent Technologies, United States; [2]Stanford University, United States

17:10 **An Integrated 80-V Class-D Power Output Stage with 94% Efficiency in a 0.14µm SOI BCD Process**
Haifeng Ma, Ronan van der Zee, Bram Nauta
University of Twente, Netherlands

17:30 **A 443-µA 37.8-nV/Sqrt(Hz) CMOS Multi-Stage Bandgap Voltage Reference**
Weixun Yan, Thomas Christen
ams AG, Switzerland

17:50 **A 0.25-µm CMOS, 7-ppm/°C, 8-µA Quiescent Current, ±5-mA Output Current Low-Dropout Voltage Regulator**
Fabrizio Conso[2], Gabriele Rescio[2], Marco Grassi[2], Calogero Ribellino[1], Giuseppina Billè[1], Alessandro Rizzo[1], Sandor Petenyi[1], Salvo Privitera[1], Piero Malcovati[2]
[1]STMicroelectronics, Italy; [2]Università degli studi di Pavia, Italy

18:10 **A 40 nm LP CMOS Self-Biased Continuous-Time Comparator with Sub-100ps Delay at 1.1V & 1.2mW**
Vladimir Milovanovic, Horst Zimmermann
Vienna University of Technology, Austria

18:30 **On-Chip Temperature Compensation of Driver Voltage for LC-Displays**
Rolf Becker, Aleksandar Zhelyazkov, Bernie Kim
NXP Semiconductors, Switzerland

Tuesday, September 17

Nyquist Rate ADCs

Session Code: A6L-B
Location: Room B
Date & Time: Tuesday, September 17
16:50 - 18:50
Chair(s): Georgi Radulov
T. Univ. Eindhoven
George Gielen
K. U. Leuven

16:50 **A 12b 50MS/s 2.1mW SAR ADC with Redundancy and Digital Background Calibration**
Albert Chang, Hae-Seung Lee, Duane Boning
Massachusetts Institute of Technology, United States

17:10 **A Low Power Zero-Crossing Pipeline-SAR ADC with on-Chip Dynamically Loaded Pre-Charged Reference**
Jayanth Kuppambatti, Peter Kinget
Columbia University, United States

17:30 **An 8-bit 450-MS/s Single-bit/Cycle SAR ADC in 65-nm CMOS**
Vaibhav Tripathi, Boris Murmann
Stanford University, United States

17:50 **An 11b 1GS/s ADC with Parallel Sampling Architecture to Enhance SNDR for Multi-Carrier Signals**
Yu Lin[2], Kostas Doris[2], Erwin Janssen[2], Athon Zanikopoulos[2], Alessandro Murroni[2], Gerard van der Weide[2], Hans Hegt[1], Arthur H.M. van Roermund[1]
[1]Eindhoven University of Technology, Netherlands; [2]NXP Semiconductors, Netherlands

18:10 **A 9b 2GS/s 45mW 2X-Interleaved ADC**
Jorge Pernillo, Michael Flynn
University of Michigan, United States

18:30 **A 6-bit 6-GS/s 95mW Background Calibrated Flash ADC with Integrating Preamplifiers and Half-Rate Comparators in 32nm LP CMOS**
Francesco Radice[3], Melchiorre Bruccoleri[3], Marcello Ganzerli[2], Giorgio Spelgatti[1], Davide Sanzogni[3], Massimo Pozzoni[3], Andrea Mazzanti[4]
[1]Marvell Semiconductors, Italy; [2]NXP Semiconductors, Netherlands; [3]STMicroelectronics, Italy; [4]Università degli studi di Pavia, Italy

Tuesday, September 17

Biomedical Circuits & Systems

Session Code: A6L-C

Location: Room C

Date & Time: Tuesday, September 17
16:50 - 18:50

Chair(s): Andreas Demosthenous
University College London
Firat Yazicioglu
IMEC

16:50 **A 78 pW 1 b/s 2.4 GHz Radio Transmitter for Near-Zero-Power Sensing Applications**
Patrick Mercier[4], Saurav Bandyopadhyay[3], Andrew Lysaght[2], Konstantina Stankovic[1], Anantha Chandrakasan[3]
[1]Harvard Medical School, United States; [2]Massachusetts Eye and Ear Infirmary, United States; [3]Massachusetts Institute of Technology, United States; [4]University of California, San Diego, United States

17:10 **A 0.13µm CMOS Integrated Wireless Power Receiver for Biomedical Applications**
Meysam Zargham, P.Glenn Gulak
University of Toronto, Canada

17:30 **85 dB Dynamic Range 1.2 mW 156 kS/s Biopotential Recording IC for High-Density ECoG Flexible Active Electrode Array**
Sohmyung Ha[3], Jongkil Park[3], Yu Chi[1], Jonathan Viventi[2], John Rogers[4], Gert Cauwenberghs[3]
[1]Cognionics, Inc., United States; [2]Polytechnic Institute of New York University, United States; [3]University of California, San Diego, United States; [4]University of Illinois at Urbana-Champaign, United States

17:50 **A 14 µA ECG Processor with Robust Heart Rate Monitor for a Wearable Healthcare System**
Shintaro Izumi[1], Ken Yamashita[1], Masanao Nakano[1], Toshihiro Konishi[1], Hiroshi Kawaguchi[1], Hiromitsu Kimura[4], Kyoji Marumoto[4], Takaaki Fuchikami[4], Yoshikazu Fujimori[4], Hiroshi Nakajima[2], Toshikazu Shiga[3], Masahiko Yoshimoto[1]
[1]Kobe University, Japan; [2]Omron Corporation, Japan; [3]Omron Healthcare Inc., Japan; [4]Rohm Co. Ltd., Japan

18:10 **A DC-Connectable Multi-Channel Biomedical Data Acquisition ASIC with Mains Frequency Cancellation**
Philipp Schönle[1], Felix Schulthess[1], Schekeb Fateh[1], Roger Ulrich[3], Fiona Huang[2], Thomas Burger[1], Qiuting Huang[1]
[1]ETH Zürich, Switzerland; [2]Integrated Systems Laboratory, ETH Zurich, Switzerland; [3]Kandou Bus, Switzerland

Tuesday, September 17

Power Converters and Drivers

Session Code: A6L-D

Location: Room D

Date & Time: Tuesday, September 17
16:50 - 18:30

Chair(s): Bernhard Wicht
Reutlingen University
Michael Mark
Infineon

16:50 **94.6% Peak Efficiency DCM Buck Converter with Fast Adaptive Dead-Time Control**
Sujan Manohar, Poras Balsara
University of Texas at Dallas, United States

17:10 **Switching-Based Charger with Continuously Built-in Resistor Detector (CBIRD) and Analog Multiplication-Division Unit (AMDU) for Fast Charging in Li-Ion Battery**
Ruei-Hong Peng[4], Tsu-Wei Tsai[4], Ke-Horng Chen[4], Zhih Han Tai[1], Yi Hsuan Cheng[1], Chi Chung Tsai[1], Hsin-Yu Luo[3], Shih-Ming Wang[2], Long-Der Chen[2], Cheng-Chen Yang[2], Jui-Lung Chen[5]
[1]Chunghwa Picture Tubes, Ltd., Taiwan; [2]Industrial Technology Research Institute, Taiwan; [3]Metal Industries Research & Development Centre, Taiwan; [4]National Chiao Tung University, Taiwan; [5]Vanguard International Semiconductor Corp., Taiwan

17:30 **An Integrated Ultracapacitor Fast Mains Charger with Combined Power/Current Optimisation**
Rares Bodnar, William Redman-White
University of Southampton, United Kingdom

17:50 **A Monolithic Stacked Class-D Approach for High Voltage DC-AC Conversion in Standard CMOS**
Piet Callemeyn, Michiel Steyaert
Katholieke Universiteit Leuven, Belgium

18:10 **A 0.18-µm CMOS, -92-dB THD, 105-dBA DR, Third-Order Audio Class-D Amplifier**
Davide Cartasegna[1], Piero Malcovati[3], Lorenzo Crespi[1], Andrea Baschirotto[2]
[1]Conexant Systems, United States; [2]Università degli Studi di Milano - Bicocca, Italy; [3]Università degli studi di Pavia, Italy

Wednesday, September 18

RF Receivers and Front-ends

Session Code: B3L-A
Location: Room A
Date & Time: Wednesday, September 18
10:50 - 12:30
Chair(s): Marc Borremans
Telenet
Paul Muller
MediaTek Inc.

10:50 **Dual-Band RF Receiver for GPS and Compass Systems in 55-nm CMOS**
Songting Li, Jiancheng Li, Xiaochen Gu, Hongyi Wang, Jianfei Wu, Dun Yan, Zhaowen Zhuang
National University of Defense Technology, China

11:10 **A 180nm Fully-Integrated Dual-Channel Reconfigurable Receiver for GNSS Interoperations**
Nan Qi, Baoyong Chi, Yang Xu, Zhou Chen, Yang Xu, Jun Xie, Zheng Song, Zhihua Wang
Tsinghua University, China

11:30 **A 0.9GHz-5.8GHz SDR Receiver Front-End with Transformer-Based Current-Gain Boosting and 81-dB 3rd-Order-Harmonic Rejection Ratio**
Alan Wing Lun Ng, S.Y. Zheng, H. Leung, Y. Chao, Howard Luong
Hong Kong University of Science and Technology, Hong Kong

11:50 **An RF Receiver with an Integrated Adaptive Notch Filter for Multi-Standard Applications**
Ashkan Borna[3], Chris Hull[2], Yanjie Wang[2], Hua Wang[1], Ali Niknejad[3]
[1]Georgia Institute of Technology, United States; [2]Intel, United States; [3]University of California, Berkeley, United States

12:10 **A 2.14GHz Watt-Level Power Amplifier with Passive Load Modulation in a SOI CMOS Technology**
Gauthier Tant[1], Alexandre Giry[1], Pierre Vincent[1], Jean-Daniel Arnould[2], Jean-Michel Fournier[2]
[1]CEA-LETI, France; [2]IMEP-LAHC, France

Wednesday, September 18

Memories

Session Code: B3L-B

Location: Room B

Date & Time: Wednesday, September 18
10:50 - 12:30

Chair(s): Sylvain Clerc
ST Microelectronics
Ralph Hasholzner
Intel Corporation

10:50 **A 65nm 4MB Embedded Flash Macro for Automotive Achieving a Read Throughput of 5.7GB/s and a Write Throughput of 1.4MB/s**
Mihail Jefremow[2], Thomas Kern[1], Ulrich Backhausen[1], Johannes Elbs[1], Benoit Rousseau[1], Christoph Roll[1], Leonardo Castro[1], Thomas Roehr[1], Edvin Paparisto[1], Kirk Herfurth[1], Rainer Bartenschlager[1], Stefanie Thierold[1], Roland Renardy[1]
[1]Infineon Technologies AG, Germany; [2]Infineon Technologies AG / Technische Universität München, Germany; [3]Technische Universität München, Germany

11:10 **Dual-VT 4kb Sub-VT Memories with <1 pW/bit Leakage in 65 nm CMOS**
Oskar Andersson[2], Babak Mohammadi[2], Pascal Meinerzhagen[1], Andreas Burg[1], Joachim Neves Rodrigues[2]
[1]École Polytechnique Fédérale de Lausanne, Switzerland; [2]Lund University, Sweden

11:30 **A 40 nm, 454MHz 114 fJ/bit Area-Efficient SRAM Memory with Integrated Charge Pump**
Bram Rooseleer, Wim Dehaene
Katholieke Universiteit Leuven, Belgium

11:50 **Scalable 0.35V to 1.2V SRAM Bitcell Design from 65nm CMOS to 28nm FDSOI**
Fady Abouzeid, Audrey Bienfait, Kaya Can Akyel, Sylvain Clerc, Lorenzo Ciampolini, Philippe Roche
STMicroelectronics, France

12:10 **Design of a Power-Efficient Cam Using Automated Background Checking Scheme for Small Match Line Swing**
Anh Tuan Do, Chun Yin, Kiat Seng Yeo, Tony Tae-Hyoung Kim
Nanyang Technological University, Singapore

Wednesday, September 18

Magnetic, Temperature and Pressure Sensors

Session Code: B3L-C

Location: Room C

Date & Time: Wednesday, September 18
10:50 - 12:30

Chair(s): Hanspeter Schmid
Univ. of Applied Sciences & Arts Northwestern Switzerland
Werner Brockherde
Fraunhofer

10:50 **A Dual Vertical Hall Latch with Direction Detection**
Dan Stoica[2], Mario Motz[1]
[1]Infineon Technologies Austria AG, Austria; [2]Infineon Technologies Romania SCS, Romania

11:10 **A Continuous-Time Ripple Reduction Technique for Spinning-Current Hall Sensors**
Junfeng Jiang[1], Kofi A.A. Makinwa[1], Wilko Kindt[2]
[1]Technische Universiteit Delft, Netherlands; [2]Texas Instruments Holland B.V., Netherlands

11:30 **A 40µW CMOS Temperature Sensor with an Inaccuracy of ±0.4°C (3-Sigma) from -55°C to 200°C**
Kamran Souri, Kianoush Souri, Kofi A.A. Makinwa
Technische Universiteit Delft, Netherlands

11:50 **A Resistor-Based Temperature Sensor for MEMS Frequency References**
Mina Shahmohammadi, Kianoush Souri, Kofi A.A. Makinwa
Technische Universiteit Delft, Netherlands

12:10 **128 Nodes 4.5 mm Pitch 15-bit Pressure Sensor Ribbon**
Cyril Condemine[1], Jerome Willemin[1], Sylvain Bouquet[1], Stephanie Robinet[1], Antoine Robinet[1], Laurent Jouanet[1], Guillaume Regis[2], Olivier Compagnon[2], Sully Vitry[2]
[1]CEA-LETI, France; [2]MIND Mircotec, France

Wednesday, September 18

Frequency Synthesis

Session Code: B3L-D
Location: Room D
Date & Time: Wednesday, September 18
10:50 - 12:10
Chair(s): Pietro Andreani
Lund University
Jan Crols
Ansem

10:50 **An Injection-Locking Based Programmable Fractional Frequency Divider with 0.2 Division Step for Quantization Noise Reduction**
Raghavasimhan Thirunarayanan[3], David Ruffieux[1], Christian Enz[2]
[1]CSEM, Switzerland; [2]École Polytechnique Fédérale de Lausanne, Switzerland; [3]École Polytechnique Fédérale de Lausanne & CSEM, Switzerland

11:10 **A 0.3-to-8.5 GHz Frequency Synthesizer Based on Digital Period Synthesis**
Tapio Rapinoja, Kari Stadius, Jussi Ryynänen
Aalto University, Finland

11:30 **Frequency Translation Through Fractional Division for a Two-Channel Pulling Mitigation**
Seyed Amir Reza Ahmadi Mehr, Massoud Tohidian, Robert Bogdan Staszewski
Technische Universiteit Delft, Netherlands

11:50 **High Speed, High Accuracy Fractional-N Frequency Synthesizer Using Nested Mixed-Radix Digital Delta-Sigma Modulators**
Michael Peter Kennedy[3], Brian Fitzgibbon[2], Austin Harney[1], Hyman Shanan[1], Mike Keaveney[1]
[1]Analog Devices, Ireland; [2]Susquehanna International, Ireland; [3]University College Cork, Ireland

Wednesday, September 18

ESSCIRC Keynote: B. Murmann (Stanford Univ.)

Session Code: B4L-E

Location: Room CT

Date & Time: Wednesday, September 18
14:00 - 15:00

Chair(s): Andrea Baschirotto
Università del Salento

14:00 **Digitally Assisted Data Converter Design**
Boris Murmann
Stanford University, United States

Wednesday, September 18

ESSCIRC Invited Session on Emerging Technology

Session Code: B5L-E
Location: Room CT
Date & Time: Wednesday, September 18
15:00 - 16:00
Chair(s): Edoardo Charbon
TU Delft

15:00 **Solid State RF MEMS Resonators in Standard CMOS**
Bichoy Bahr, Radhika Marathe, Wentao Wang, Dana Weinstein
Massachusetts Institute of Technology, United States

15:20 **Oxide Electronics for Imaging and Displays**
Arokia Nathan, Sungsik Lee, Sanghun Jeon
University of Cambridge, United Kingdom

15:40 **Why Design Reliable Chips When Faulty Ones Are Even Better**
Krishna V. Palem[3], Avinash Lingamneni[3], Christian Enz[2], Christian Piguet[1]
[1]CSEM, Switzerland; [2]École Polytechnique Fédérale de Lausanne, Switzerland; [3]Rice University, United States

Wednesday, September 18

Application-specific Processors & Circuits

Session Code: B6L-D

Location: Room D

Date & Time: Wednesday, September 18
16:30 - 17:50

Chair(s): Stefan Rusu
Intel Corporation
Marian Verhelst
KU Leuven

16:30 **A High-Throughput 16x Super Resolution Processor for Real-Time Object Recognition SoC**
Junyoung Park[2], Byeong-Gyu Nam[1], Hoi-Jun Yoo[2]
[1]Chungnam National University, Korea, South; [2]Korea Advanced Institute of Science and Technology, Korea, South

16:50 **Cross-Layer Optimization of QRD Accelerators**
Upasna Vishnoi, Tobias Noll
Rheinisch-Westfälische Technische Hochschule Aachen, Germany

17:10 **Word-Parallel Coprocessor Architecture for Digital Nearest Euclidean Distance Search**
Toshinobu Akazawa, Seiryu Sasaki, Hans Juergen Mattausch
Hiroshima University, Japan

17:30 **In-Situ Performance Monitor Employing Threshold Based Notifications (TheBaN)**
Tobias Gemmeke, Mario Konijnenburg, Christian Bachmann
Holst Centre / imec, Netherlands

Wednesday, September 18

RF Transceiver Circuits

Session Code: B6L-E

Location: Room CT

Date & Time: Wednesday, September 18
16:30 - 17:50

Chair(s): Jussi Ryynanen
Aalto University
Peter Baltus
Eindhoven University of Technology

16:30 **A 0.4 GHz - 4 GHz Direct RF-to-Digital Sigma-Delta Multi-Mode Receiver**
Charles Wu, Borivoje Nikolic
University of California, Berkeley, United States

16:50 **A 0.7 - 3.7 GHz Six Phase Receiver Front-End with Third Order Harmonic Rejection**
Anders Nejdel, Markus Törmänen, Henrik Sjöland
Lund University, Sweden

17:10 **A Low Out-of-Band Noise LTE Transmitter with Current-Mode Approach**
Nicola Codega[1], Antonio Liscidini[2], Rinaldo Castello[1]
[1]Università degli studi di Pavia, Italy; [2]University of Toronto, Canada

17:30 **A 39 dB DR CMOS Log-Amp RF Power Detector with ± 1.1 dB Temperature Drift from -40 to 85°C**
Eric Muijs[2], Paulo Silva[3], Arie van Staveren[3], Wouter Serdijn[1]
[1]Technische Universiteit Delft, Netherlands; [2]Technische Universiteit Delft & Texas Instruments, Netherlands; [3]Texas Instruments, Netherlands

Wednesday, September 18

CMOS Image Sensors

Session Code: B6L-F

Location: Room TM

Date & Time: Wednesday, September 18
16:30 - 17:50

Chair(s): Angel Rodriguez-Vazquez
University of Sevilla
Johannes Solhusvik
Omnivision

16:30 **2x(4x)128 Time-Gated CMOS Single Photon Avalanche Diode Line Detector with 100 Ps Resolution for Raman Spectroscopy**
Ilkka Nissinen, Antti-Kalle Länsman, Jan Nissinen, Jouni Holma, Juha Kostamovaara
University of Oulu, Finland

16:50 **Compact Analog Counting SPAD Pixel with 1.9% PRNU and 530ps Time Gating**
Lucio Pancheri[2], Ekaterina Panina[2], Gian-Franco Dalla Betta[2], Leonardo Gasparini[1], David Stoppa[1]
[1]Fondazione Bruno Kessler, Italy; [2]Università degli Studi di Trento, Italy

17:10 **Speed Considerations for LDPD Based Time-of-Flight CMOS 3D Image Sensors**
Andreas Süss[1], Christian Nitta[1], Andreas Spickermann[1], Daniel Durini[1], Gabor Varga[2], Melanie Jung[1], Werner Brockherde[1], Bedrich J. Hosticka[1], Holger Vogt[1], Stefan Schwope[3]
[1]Fraunhofer IMS, Germany; [2]Rheinisch-Westfälische Technische Hochschule Aachen, Germany; [3]TriDiCam, Germany

17:30 **A 80µW 30fps 104 x 104 All-nMOS Pixels CMOS Imager with 7-bit PWM ADC for Robust Detection of Relative Intensity Change**
Michele Benetti[2], Massimo Gottardi[2], Zeev Smilansky[1]
[1]Emza Visual Sense Ltd., Israel; [2]Fondazione Bruno Kessler, Italy

Thursday, September 19

ESSCIRC Keynote: P. Kinget (Columbia Univ.)

Session Code: C3L-E

Location: Room CT

Date & Time: Thursday, September 19
11:20 - 12:20

Chair(s): Peter Mole
Intersil

11:20 **Scaling Analog Circuits**
Peter Kinget, Jayanth Kuppambatti, Baradwaj Vigraham, Chun-Wei Hsu
Columbia University, United States

Thursday, September 19

Analog II

Session Code: C4L-A

Location: Room A

Date & Time: Thursday, September 19
14:00 - 15:00

Chair(s): Boris Murmann
Stanford University
Hugo Veenstra
Philips

14:00 **A 40nm-CMOS, 72µW Injection-Locked Timing Reference and 1.8 Mbit/s Coordination Receiver for Wireless Sensor Networks**
Valentijn De Smedt[2], Georges Gielen[1], Wim Dehaene[1]
[1]Katholieke Universiteit Leuven, Belgium; [2]Technische Universiteit Delft, Belgium

14:20 **High-Resolution and Wide-Dynamic Range Time-to-Digital Converter with a Multi-Phase Cyclic Vernier Delay Line**
Mino Kim[2], Woo-Yeol Shin[3], Gi-Moon Hong[2], Jihwan Park[2], Joo-Hyung Chae[2], Nan Xing[1], Jong-Kwan Woo[4], Suhwan Kim[2]
[1]Samsung, Korea, South; [2]Seoul National University, Korea, South; [3]SK Hynix, Korea, South; [4]University of Michigan, United States

14:40 **A 32.55-kHz, 472-nW, 120ppm/°C, Fully on-Chip, Variation Tolerant CMOS Relaxation Oscillator for a Real-Time Clock Application**
Keishi Tsubaki, Tetsuya Hirose, Nobutaka Kuroki, Masahiro Numa
Kobe University, Japan

Thursday, September 19

Oversampled ADCs I

Session Code: C4L-B

Location: Room B

Date & Time: Thursday, September 19
14:00 - 15:00

Chair(s): Lucien Breems
NXP
Angelo Nagari
ST-Ericsson

14:00 **A 0.039mm² Inverter-Based 1.82mW 68.6dB-SNDR 10MHz-BW CT-Sigma-Delta-ADC in 65nm CMOS**
Sebastian Zeller[1], Christian Muenker[3], Robert Weigel[2]
[1]Consultant, Germany; [2]Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; [3]University of Applied Sciences Munich, Germany

14:20 **A 9MHz Filtering ADC with Additional 2nd-Order Delta-Sigma Modulator Noise Suppression**
Mattias Andersson[2], Martin Anderson[1], Lars Sundström[1], Sven Mattisson[1], Pietro Andreani[2]
[1]Ericsson AB, Sweden; [2]Lund University, Sweden

14:40 **A 40MHz-BW Two-Step Open-Loop VCO-Based ADC with 42fJ/Step FoM in 40nm CMOS**
Xinpeng Xing, Peng Gao, Georges Gielen
Katholieke Universiteit Leuven, Belgium

Thursday, September 19

Millimeter-wave Circuits

Session Code: C4L-C

Location: Room C

Date & Time: Thursday, September 19
14:00 - 15:00

Chair(s): Sven Mattisson
Ericsson
Peter Kennedy
University College Cork

14:00 **A 120GHz Fully Integrated 10Gb/s Wireless Transmitter with on-Chip Antenna in 45nm Low Power CMOS**
Noël Deferm[1], Wouter Volkaerts[1], Juan Osorio[2], Anton de Graauw[2], Michiel Steyaert[1], Patrick Reynaert[1]
[1]Katholieke Universiteit Leuven, Belgium; [2]NXP Semiconductors, Netherlands

14:20 **A Plastic Waveguide Receiver in 40nm CMOS with on-Chip Bondwire Antenna**
Maarten Tytgat, Patrick Reynaert
Katholieke Universiteit Leuven, Belgium

14:40 **A 1-V 1.25-Gbps CMOS Analog Front-End for Short Reach Optical Links**
Cecilia Gimeno, Carlos Sánchez-Azqueta, Erick Guerrero, Concepción Aldea, Santiago Celma
Universidad de Zaragoza, Spain

Thursday, September 19

LED/LCD Drivers

Session Code: C4L-D

Location: Room D

Date & Time: Thursday, September 19
14:00 - 15:00

Chair(s): Michiel Steyaert
KULeuven
Philip Mok
The Hong Kong University of Science & Technology

14:00 **Integrated Buck LED Driver with Application Specific Digital Architecture**
Giovanni Capodivacca, Paolo Milanesi, Andrea Scenini
Infineon Technologies Italia, Italy

14:20 **Variable off Time Current - Mode Floating Buck Controller - a Different Approach**
Vlad Anghel[1], Chris Bartholomeusz[1], Gheorghe Pristavu[2], Gheorghe Brezeanu[2]
[1]ON Semiconductor, United States; [2]Universitatea Politehnica din Bucuresti, Romania

14:40 **Embedded Fully Self-Biased Switched-Capacitor for Energy and Area-Efficient Cholesteric LCD Drivers**
Wen-Shen Chou[4], Po-Hsien Huang[4], Ming-Yan Fan[4], Ke-Horng Chen[4], Kuei-Ann Wen[4], Zhih Han Tai[1], Yi Hsuan Cheng[1], Chi Chung Tsai[1], Hsin-Yu Luo[3], Shih-Ming Wang[2], Long-Der Chen[2], Cheng-Chen Yang[2], Jui-Lung Chen[5]
[1]Chunghwa Picture Tubes, Ltd., Taiwan; [2]Industrial Technology Research Institute, Taiwan; [3]Metal Industries Research & Development Centre, Taiwan; [4]National Chiao Tung University, Taiwan; [5]Vanguard International Semiconductor Corp., Taiwan

Thursday, September 19

Analog III

Session Code: C5L-A

Location: Room A

Date & Time: Thursday, September 19
15:00 - 16:00

Chair(s): Peter Mole
Intersil
Willy Sansen
KU Leuven ESAT-MICAS

15:00 **A 4 a Peak Current and 2 Ns Pulse Width CMOS Laser Diode Driver for High Measurement Rate Applications**
Jan Nissinen, Juha Kostamovaara
University of Oulu, Finland

15:20 **High Temperature Analog Circuit Design in PD-SOI CMOS Technology Using Reverse Body Biasing**
Alexander Schmidt, Holger Kappert, Rainer Kokozinski
Fraunhofer IMS, Germany

15:40 **EMC Compliant LIN Transceiver**
Philipp Schröter[2], Magnus-Maria Hell[2], Martin Frey[1]
[1]IC Design consultant working for Infineon, Germany;
[2]Infineon Technologies AG, Germany

Thursday, September 19

Oversampled ADCs II

Session Code: C5L-B

Location: Room B

Date & Time: Thursday, September 19
15:00 - 16:00

Chair(s): Claudius Dan
University Politehnica Bucharest
Piero Malcovati
University of Pavia

15:00 **A 1-V 99-to-75dB SNDR, 256Hz-16kHz Bandwidth, 8.6-to-39µW Reconfigurable SC Sigma-Delta Modulator for Autonomous Biomedical Applications**
Serena Porrazzo[1], Venkata Narasimha Manyam[2], Alonso Morgado[3], David San Segundo Bello[2], Chris Van Hoof[3], Arthur H.M. van Roermund[1], Refet Firat Yazicioglu[2], Eugenio Cantatore[1]
[1]Eindhoven University of Technology, Netherlands; [2]Imec, Belgium; [3]Imec & Katholieke Universiteit Leuven, Belgium

15:20 **A 105-dB SNDR, 10 kSps Multi-Level Second-Order Incremental Converter with Smart-DEM Consuming 280 µW and 3.3-V Supply**
Yao Liu[3], Edoardo Bonizzoni[2], Alessandro D'Amato[1], Franco Maloberti[2]
[1]Texas Instruments, Italy; [2]Università degli studi di Pavia, Italy; [3]University of Pavia, Italy

15:40 **A 0.1-mm² 3-Channel Area-Optimized Sigma-Delta ADC in 0.16-µm CMOS with 20-kHz BW and 86-dB DR**
Fabio Sebastiano[2], Robert van Veldhoven[1]
[1]NXP Semiconductore, Netherlands; [2]NXP Semiconductors, Netherlands

Thursday, September 19

Wake-up Receivers

Session Code: C5L-C

Location: Room C

Date & Time: Thursday, September 19
15:00 - 16:00

Chair(s): Frank Op't Eynde
Audax Technologies
Jan Craninckx
IMEC

15:00 **A 35 pJ/Pulse Injection-Locking Based UWB Transmitter for Wirelessly-Powered RFID Tags**
Jia Mao, Zhuo Zou, Lirong Zheng
KTH Royal Institute of Technology, Sweden

15:20 **60-GHz, 9-µW Wake-Up Receiver for Short-Range Wireless Communications**
Toshiki Wada, Masayuki Ikebe, Eiichi Sano
Hokkaido University, Japan

15:40 **A 3-µW 868-MHz Wake-Up Receiver with -83 dBm Sensitivity and Scalable Data Rate**
Heinrich Milosiu, Frank Oehler, Markus Eppel, Dieter Frühsorger, Stephan Lensing, Gralf Popken, Thomas Thönes
Fraunhofer IIS, Germany

Thursday, September 19

Voltage Regulators and Energy Harvesting

Session Code: C5L-D
Location: Room D
Date & Time: Thursday, September 19
15:00 - 16:00
Chair(s): Marc Pastre
EPFL
Patrick Reynaert
KULeuven

15:00 **EMI Resisting Voltage Regulator with Large Signal PSR Up to 1 GHz**
Fridolin Michel, Michiel Steyaert
Katholieke Universiteit Leuven, Belgium

15:20 **A 1mV Voltage Ripple 0.97mm² Fully Integrated Low-Power Hybrid Buck Converter**
Stefan Dietrich[1], Lei Liao[1], Frank Vanselow[2], Ralf Wunderlich[1], Stefan Heinen[1]
[1]Rheinisch-Westfälische Technische Hochschule Aachen, Germany; [2]Texas Instruments Deutschland GmbH, Germany

15:40 **An Autonomous Piezoelectric Energy Harvesting IC Based on a Synchronous Multi-Shots Technique**
Pierre Gasnier[2], Jérome Willemin[1], Sébastien Boisseau[1], Ghislain Despesse[1], Cyril Condemine[1], Guillaume Gouvernet[2], Jean-Jacques Chaillout[1]
[1]CEA-LETI, France; [2]GEONAUTE Research, France

Thursday, September 19

VCOs and Dividers

Session Code: C6L-A
Location: Room A
Date & Time: Thursday, September 19
16:20 - 17:20
Chair(s): Andrea Bevilacqua
Univ. Padova
Alexandre Siligaris
CEA

16:20 **A 13.2% Locking-Range Divide-by-6, 3.1mW, ILFD Using Even-Harmonic-Enhanced Direct Injection Technique for Millimeter-Wave PLLs**
Teerachot Siriburanon, Wei Deng, Ahmed Musa, Kenichi Okada, Akira Matsuzawa
Tokyo Institute of Technology, Japan

16:40 **A High-Swing Complementary Class-C VCO**
Luca Fanori, Pietro Andreani
Lund University, Sweden

17:00 **A 0.54 THz Signal Generator in 40 nm Bulk CMOS with 22 GHz Tuning Range**
Wouter Steyaert, Patrick Reynaert
Katholieke Universiteit Leuven, Belgium

Thursday, September 19

Circuits and Systems in Emerging Technologies

Session Code: C6L-B
Location: Room B
Date & Time: Thursday, September 19
16:20 - 17:40
Chair(s): Eugenio Cantatore
TU Eindhoven
Thierry Taris
IMS

16:20 **Circuit Optimization of 4T, 6T, 8T, 10T SRAM Bitcells in 28nm UTBB FD-SOI Technology Using Back-Gate Bias Control**
Vivek Asthana, Malathi Kar, Jean Jimenez, Jean-Philippe Noel, Sebastien Haendler, Philippe Galy
STMicroelectronics, France

16:40 **Performance Impact of Through-Silicon Vias (TSVs) in Three-Dimensional Technology Measured by SRAM Ring Oscillators**
Jente B. Kuang[1], Keith Jenkins[2], K. Stawiasz[2], J. Schaub[1]
[1]IBM Austin Research Lab, United States; [2]IBM Thomas J. Watson Research Center, United States

17:00 **Design of an Organic Electronic Label on a Flexible Substrate for Temperature Sensing**
Ramkumar Ganesan[2], Jürgen Krumm[1], Sebastian Pankalla[2], Klaus Ludwig[1], Manfred Glesner[2]
[1]PolyIC GmbH & Co KG, Germany; [2]Technische Universität Darmstadt, Germany

17:20 **High Temperature-Low Temperature Coefficient Analog Voltage Reference Integrated Circuit Implemented with SiC MESFETs**
Viorel Banu, Philippe Godignon, Mihaela Alexandru, Miquel Vellvehi, Xavier Jordà, José Millán
CNM-IMB CSIC, Spain

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