High-Ohmic Resistors using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers

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Outline

- Introduction to integrated resistors
- PureB-layer integration in p⁺n diode applications
- PureB-layer resistor process flow
- Test structures and qualification parameters
- Electrical measurement results
- Conclusions
Introduction to integrated resistors

Most commonly used integrated resistors: **diffused/ implanted p- or n-type regions**

- **Resistance values ~ 1 Ω – 10 kΩ:**
  - straightforward to integrate
  - sheet resistance values ~ 10 -1000 Ω/□
  - depletion of resistor doping minimal
  - small resistor biasing dependence
  - small parasitic junction capacitance

- **Resistance values > 100 kΩ:**
  - with low sheet resistance
    - long meander resistors necessary
    - large parasitic capacitance
  - with high sheet resistance (~ 10 kΩ/□)
    - high bias dependence
    - poor doping reproducibility

[www.eet.bme.hu/~benedek/VlsiDesign/Lectures]
[www.semiconwell.com]
Introduction to integrated resistors

Pinched resistors:
- straightforward to integrate
- sheet resistance values $\sim 30 \text{k}\Omega/\square$
- small parasitic junction capacitance
  $\times$ bias dependent

Polysilicon resistors:
- lightly-doped deposited poly-silicon on oxide layer
  $\times$ non-uniform resistor value over the wafer
  $\times$ charging/discharging of defect states
  $\times$ oxide interface states cause variable resistance values

Combination of negative (polySi) and positive (c-Si) TCR resistors used to lower overall TCR. Due to process variations in both materials this is a low-yield solution. [N. Sadeghi, CCECE 2011]

[www.learnabout-electronics.org/fet_02.php]
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Pure boron chemical-vapor deposition

- CVD parameters:
  - epitaxial Si/SiGe CVD reactor
  - gas source: diborane (B₂H₆)
  - Carrier gas: hydrogen (H₂), (N₂)
  - temperatures: 500 to 700 ºC
  - lower temperature/diborane partial pressure → slower formation of PureB layer
  - constant slow growth rate, nm/min

- Properties of PureB layer:
  - high resistivity of ~ 10⁴ Ω-cm
  - chemically robust
  - does not oxidize or change in time
  - is resistant to many standard cleaning procedures

HRTEM of 700°C deposition:
Other PureB deposition properties

Under the right conditions:
• at 700ºC high selectivity to native-oxide-free Si surfaces
• uniform depositions for temperatures: 400ºC – 700ºC
• isotropic deposition on Si

Sarrubi, JEM 2009
PureB $p^+n$ forward diode characteristics

$p^+n$ diodes with n-doping $\sim 10^{17}$ cm$^{-3}$

Same behaviour for both deposition temperatures.

Behaves like conventional deep $p^+n$ junction:

near-ideal with low saturation current

Sarubbi, IEEE-TED 2010
Can use PureB layer as a vertical resistor:
- linear resistance on p-type Si
- resistivity very high but varies from run to run: $500 \times 10^4 \text{ ohm-cm}$
- easily make small mega-ohm resistors

The very high resistivity of the bulk PureB layer means that it does not play a role for the lateral sheet resistance. This is dominated by doping of the Si (700°C) or the PureB/Si interface properties (500°C).
Deposition loading effects influence thickness

Pattern-dependent thickness control $\Rightarrow$ poor vertical resistance control

Measured photodiode responsivity of low-energy electrons in e-beam set-up

[V.Mohammadi, ECS-JSSST 2012]
Sheet resistance measurements

\[ \text{Sheet resistance} \ [\Omega/\text{sq}] \]

\[ \text{Temperature} \ [\text{[°C]}] \]

\[ \sim 100 \text{ kΩ}/\square \] for low-temperature deposition or short-time deposition

Substrate doping
\[ \sim 10^{15} \text{ cm}^{-3} \]
- bias dependence saturates

Solid solubility of B in Si at 700°C
\[ = 2 \times 10^{19} \text{ cm}^{-3} \]

Sarubbi, IEEE-TED 2010
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PureB-layer resistor process flow

1) High-resistivity Si (HRS) <100> wafers n-type phosphorous-doped to 2-10 kΩ-cm

2) 200 nm thermal oxide

3) optional p-type B⁺ implanted guard ring / contact

4) window opening and PureB deposition, ~ 3 nm at 700°C or 500°C

5) 1000 nm Al deposition

6) Al dry etching with wet landing on PureB with diluted HF dip

7) Alloying in forming gas 400°C 30 min
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### Sheet resistance measurement structures

**PureB layer deposition conditions**

<table>
<thead>
<tr>
<th>Time</th>
<th>Temperature</th>
<th>Sheet resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-min</td>
<td>700°C</td>
<td>2.5×10^4 Ω/□</td>
</tr>
<tr>
<td>20-min</td>
<td>500°C</td>
<td>3.8×10^5 Ω/□</td>
</tr>
</tbody>
</table>

- **Sheet resistance**
  - 7-min 700°C: 2.5×10^4 Ω/□
  - 20-min 500°C: 3.8×10^5 Ω/□
Resistor geometries

Selection of the measured resistors

- 1000 μm by 20 μm
- 1500 μm by 20 μm
- 2000 μm by 20 μm
- 1000 μm by 10 μm
- 1500 μm by 10 μm
- 2000 μm by 10 μm
Resistor qualification parameters

- **Resistor tolerance TR** (permissible deviation from the nominal value at 25°C) is evaluated from over the wafer measurements of the average resistance $R_{av}$ inserted in the equation:

$$TR(\%) = \frac{R_i - R_{av}}{R_{av}} \times 100$$

- **Resistor voltage coefficient resistors VCR**: change in resistance with applied voltage

- **Resistor temperature coefficient TCR**: change in resistance with temperature

$$TCR \left( \frac{ppm}{^\circ C} \right) = (10^6) \frac{R-R_o}{R_o(T-T_o)}$$
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I-V characteristics of 700°C resistors

Highly linear I-V relationship $\Rightarrow$ VCR $\sim$ 0
From 85°C to 95°C the resistance value decreases slightly.
Stable under temperature cycling.
Diode leakage < 1nA/cm$^2$.
Temperature dependence of resistance

![Graph showing the temperature dependence of resistance with three different resistors at 500°C and 700°C.](image)
Temperature coefficient of the resistors

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>TCR (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>700°C</td>
<td>&lt; 400 ppm/°C</td>
</tr>
<tr>
<td>500°C</td>
<td>&lt; 200 ppm/°C</td>
</tr>
<tr>
<td></td>
<td>→ 1000 ppm/°C</td>
</tr>
</tbody>
</table>
## Resistor tolerance

Examples of the tolerance of the fabricated PureB resistors

<table>
<thead>
<tr>
<th>R(Ω)/ Die</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>R3 (kΩ)</th>
<th>R4 (kΩ)</th>
<th>R5 (MΩ)</th>
<th>R6 (MΩ)</th>
<th>R7 (MΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die 1</td>
<td>20</td>
<td>23</td>
<td>307</td>
<td>872</td>
<td>1.023</td>
<td>1.45</td>
<td>3.82</td>
</tr>
<tr>
<td>Die5</td>
<td>21</td>
<td>23.1</td>
<td>308</td>
<td>874</td>
<td>1.11</td>
<td>1.59</td>
<td>3.78</td>
</tr>
<tr>
<td>Die12</td>
<td>20</td>
<td>23</td>
<td>304</td>
<td>875</td>
<td>1.09</td>
<td>1.49</td>
<td>3.87</td>
</tr>
<tr>
<td>Average</td>
<td>20.3</td>
<td>23.03</td>
<td>306</td>
<td>873.6</td>
<td>1.07</td>
<td>1.51</td>
<td>3.82</td>
</tr>
<tr>
<td>Tolerance</td>
<td>3.2%</td>
<td>0.3%</td>
<td>0.7%</td>
<td>0.2%</td>
<td>3.3%</td>
<td>5.3%</td>
<td>1.2%</td>
</tr>
</tbody>
</table>
Conclusions

PureB resistors can be fabricated with

- sheet resistance values up to the 100 kΩ/□ range depending on deposition temperature/time in the range 500°C to 700°C,
- high linearity for all deposition temperatures,
- exceptionally low TCR, e.g. 400 ppm/°C from 15°C to 95°C, for mega-ohm resistors
- front-end CMOS compatible processing,
the PureB layer can be covered with a dielectric for protection and/or increased integration compatibility.